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Enhanced Prediction of Interconnect delays for FPGA Synthesis using MATLAB

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Outline

- Problem Statement
- Approach used to solve the problem
- Tools used
- Statistical data gathering
- Results achieved
- Key Takeaways

Introduction (1 of 3)

- Interconnect delay modeling is used early in the circuit design flow to estimate post-routed silicon delays.

- The performance of a circuit is typically dependent on parameters like wire resistance and capacitance, but approximation techniques are required to estimate timing prior to circuit layout, as these parameters are unavailable.

Introduction (2 of 3)

- Improving the accuracy of circuit delay modeling in early phases of the design process is key to producing faster circuit implementations.
- Net delay estimation strongly impacts the final result – an overly-optimistic interconnect delay model can cause bad floor planning and congestion during routing.
- An overly-pessimistic interconnect delay model can lead to chip area wastage and un-placeable design.

Introduction (3 of 3)

- In our work, we show that the *fan-out* of the nets in a circuit can be employed to guide an experimentally-derived numerical model for estimating pre-layout circuit performance.

- Prior approaches to pre-layout circuit estimation have employed simplistic functions of fan-out.

- Our approach gathers data from thousands of statistical runs of a commercial FPGA layout tool flow, then employs MATLAB to analyze the data and derive a set of high-quality, piece-wise functions which estimate pre-layout timing with strong correlation.

Approach

- Due to noise in statistical data, residual plot were used to figure out the error in data.
- Once the data is stable, smoothing is done using MATLAB.
- Final fit is obtained using curve fitting tool box.

Tools Used

- MATLAB
- Curve Fitting Tool Box
- Microsemi Libero® Place and Route Tool

Statistical Data Gathering

- Sample Output of the Statistical data obtained:

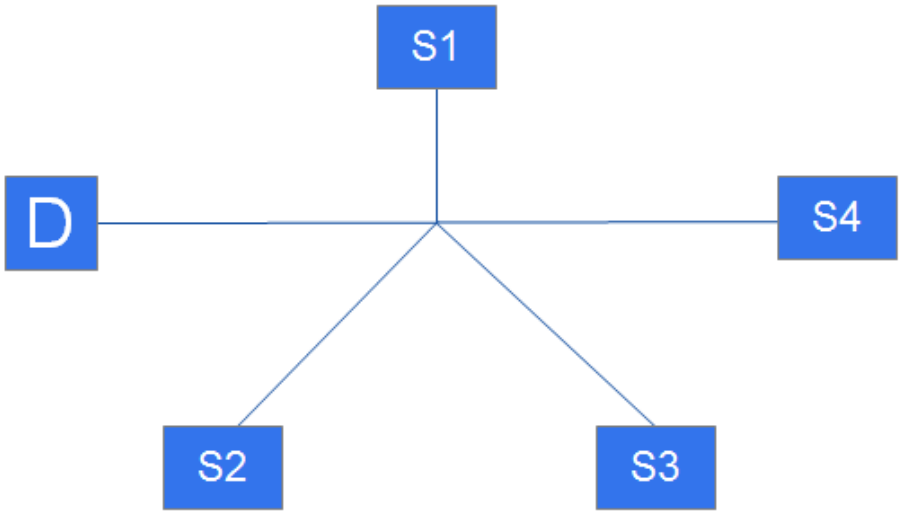
LUT	FF_D	FF_CTRL	SRAM	URAM	MATH	Delay
0	0	0	0	2	1	445
0	0	0	0	0	2	1119
0	0	0	0	0	3	2098
0	0	0	0	0	4	1920
0	0	0	0	0	5	2202
0	0	0	0	0	6	3911
0	0	0	0	0	7	4168
0	0	0	0	0	8	3979
0	0	0	0	0	9	5943

- 1st row here implies that a net driving 0 Lut pin, 0 FF:D pin, 0 FF:Ctrl pin, 0 Sram pin, 2 Uram pin and 1 Math pin is having the delay of 445ps.

- Categories:
  - DataType = LUT + FF:D
  - Control Pin Type = FF:Ctrl
  - IP Type = Sram+Uram+Math
  - IP Type1 = SRAM
  - IP Type2 = URAM
  - IP Type3 = MATH

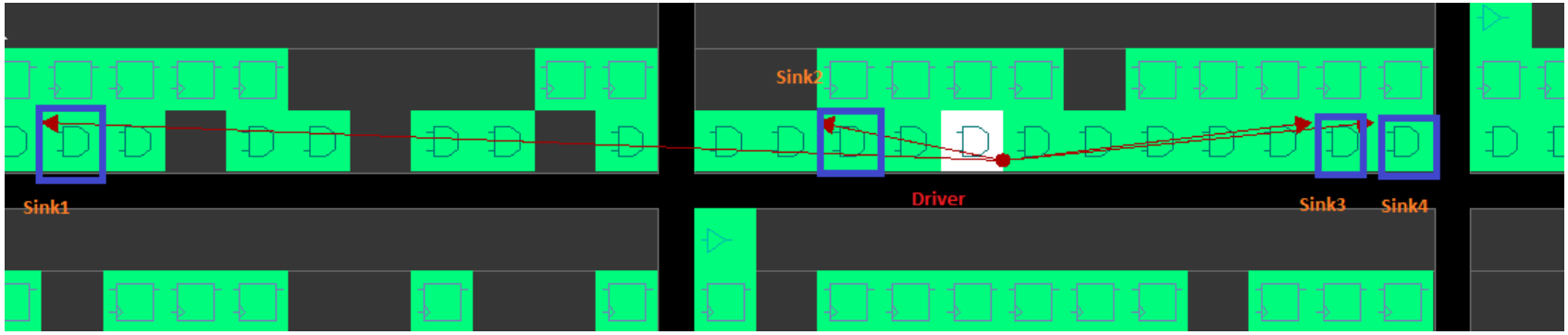
What are Fan-outs?

- The circuit netlist is represented as a graph G = (V,E), where V is a set of a circuit elements in a design and E is a set of a connections(nets) among them.
- Each net e ε E is a hyper-edge of a graph and is represented as a subset of a circuit elements, which are connected each other. Hence, |e|, the cardinality of net e, denotes the number of pins on the net.
- Figure below shows the hyper-edge with a Driver and 4 sinks. Here the Fan-out of the net is 4.



- Sample Net from a placed circuit:
- Net with a delay of 279ps is driving the input of 4 Combinatorial element(LUT).
  - Tabular representation of the statistical data for this net:

LUT	FF_D	FF_Ctrl	SRAM	URAM	MATH	Delay
4	0	0	0	0	0	279

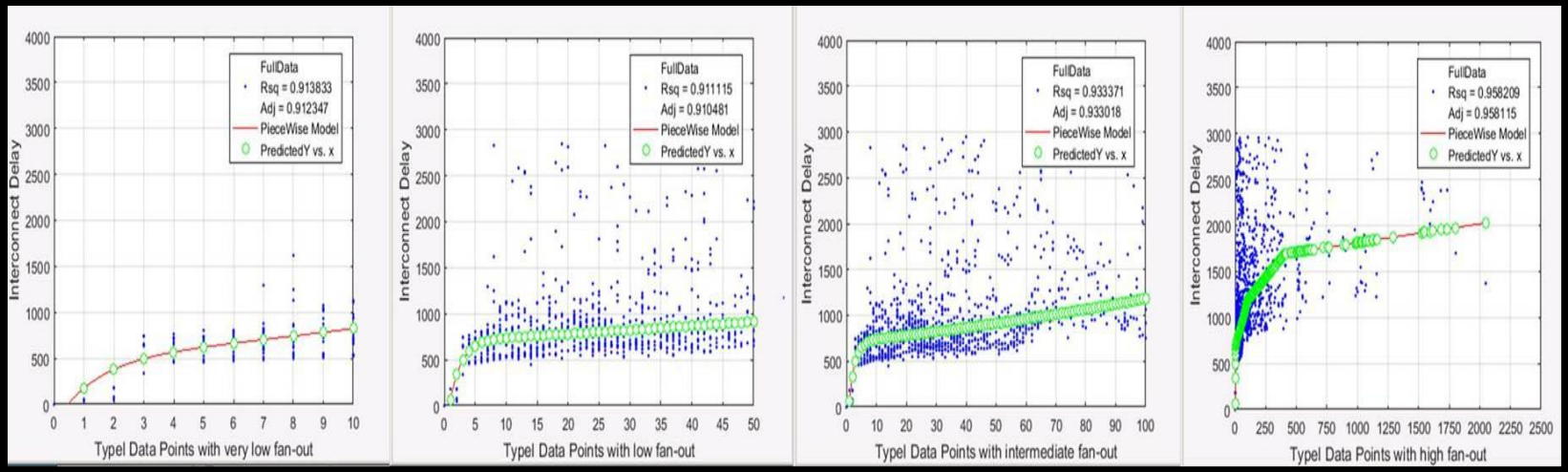


Results (1 of 7)

- Piece Wise model for our Interconnect Delays:
  - For lower fan-out, the model is two-term Exponential.
  - For intermediate fan-out, the model is linear.
  - For high fan-out, the model is linear with low slope.
- The resultant model produced a strong correlation between pre-layout & post-layout timing..

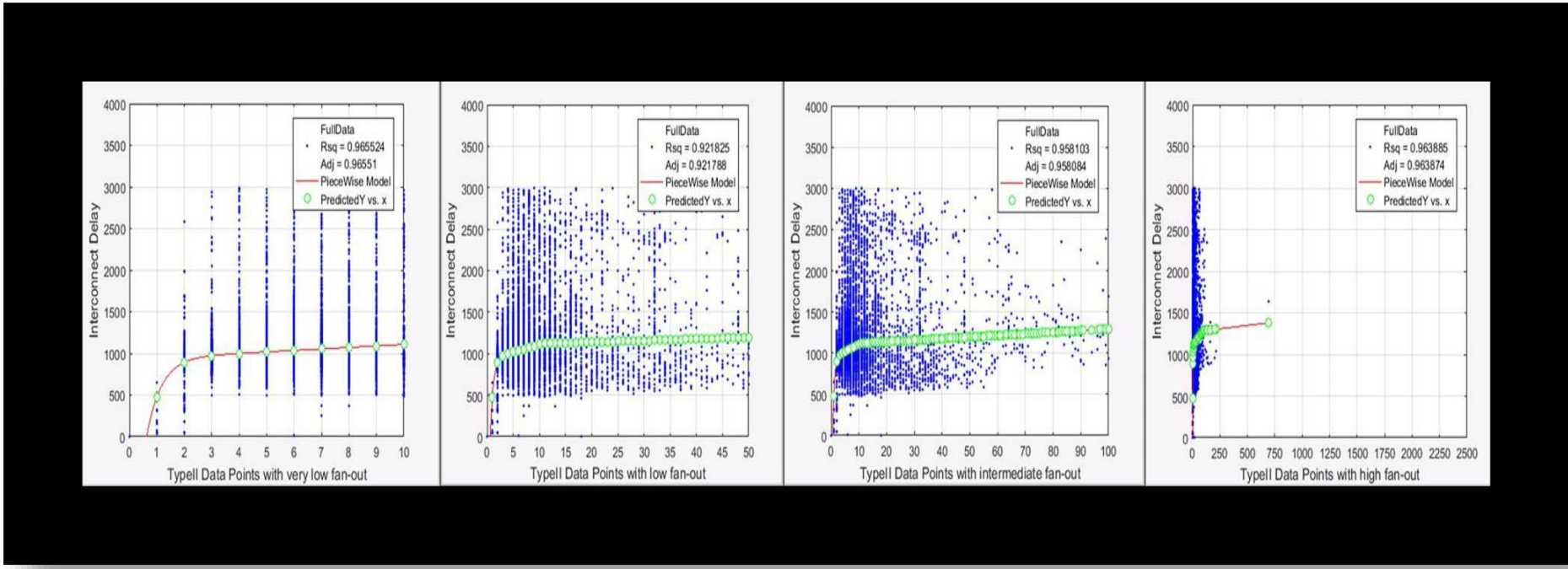
Results (2 of 7)

- Circuit delay prediction model for Type I (LUT+FF_D) Data Points:



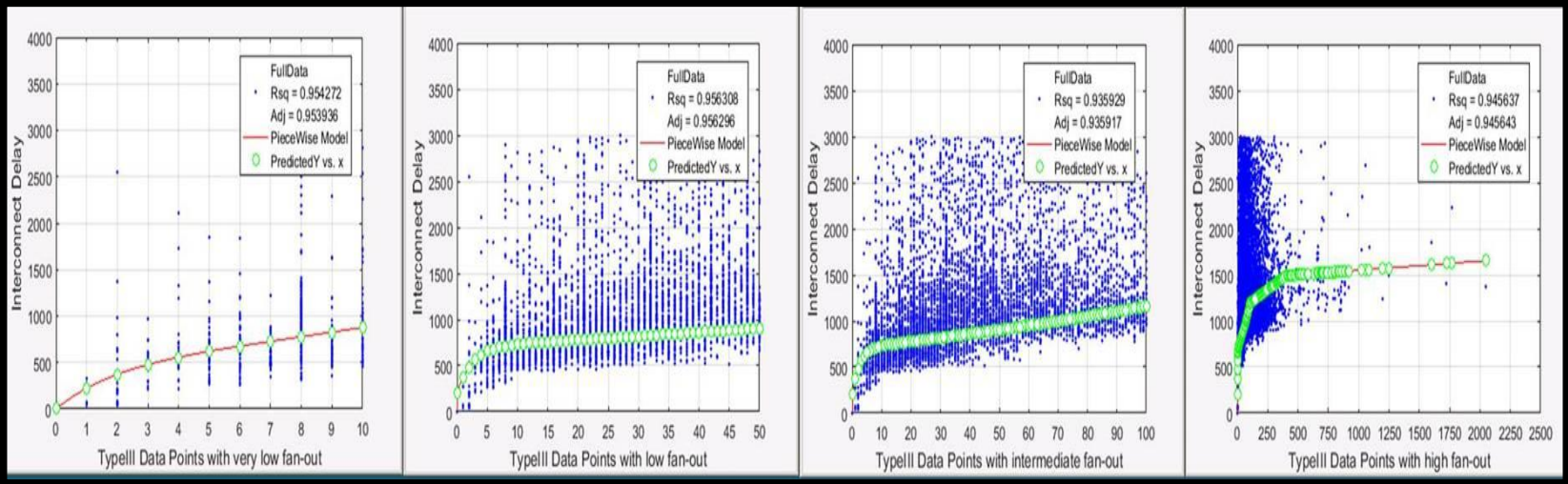
Results (3 of 7)

- Circuit delay prediction model for Type II (FF Ctrl Pins) Data Points:



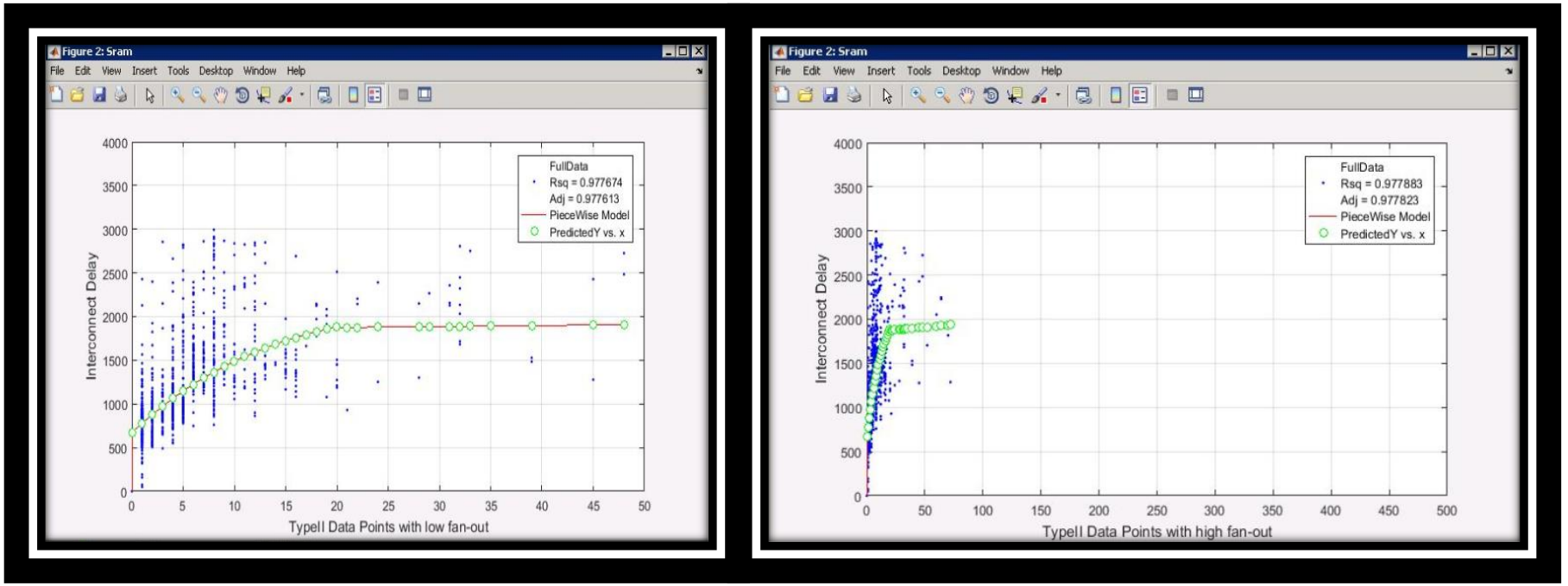
Results (4 of 7)

- Circuit delay prediction model for Type III (SRAM+URAM+MATH IP blocks) Data Points:



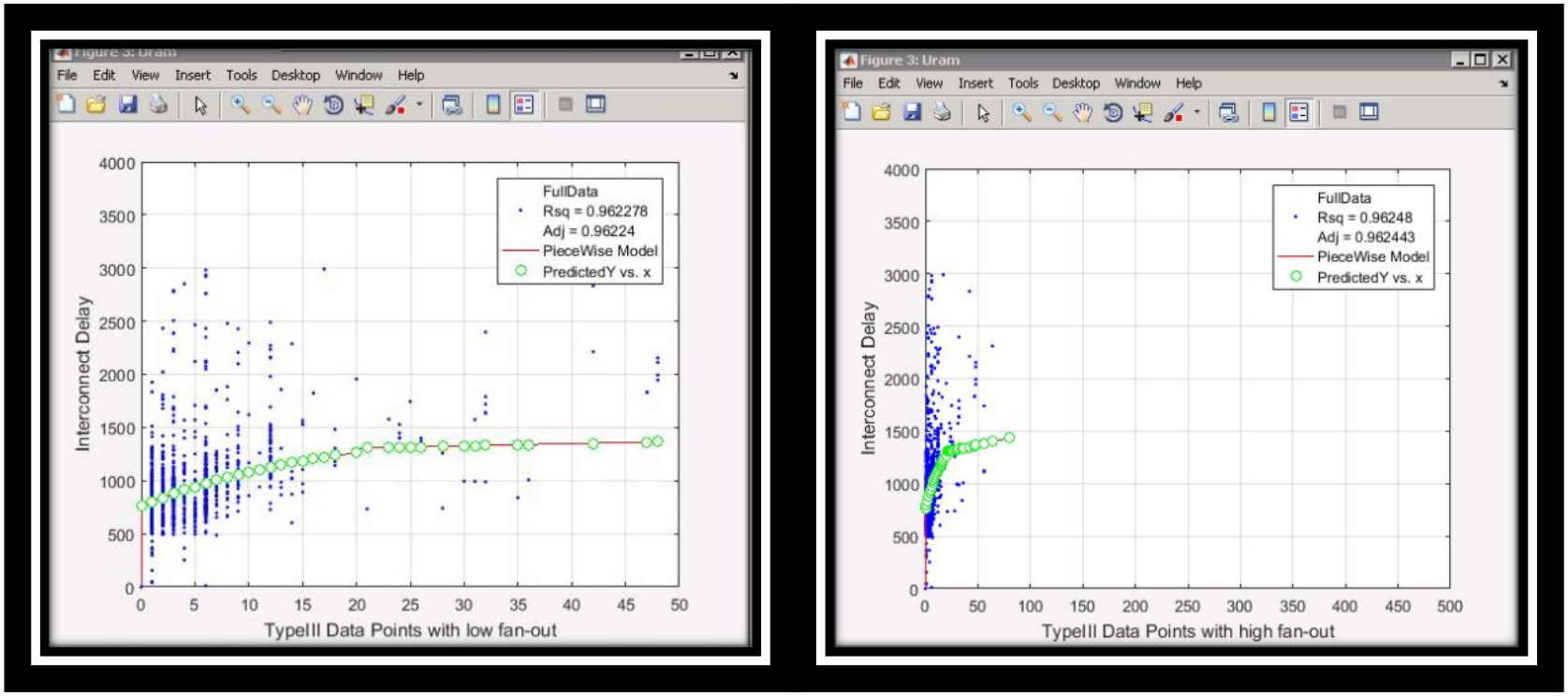
Results (5 of 7)

- Circuit delay prediction model for Type IV (SRAM IP Block) Data Points:



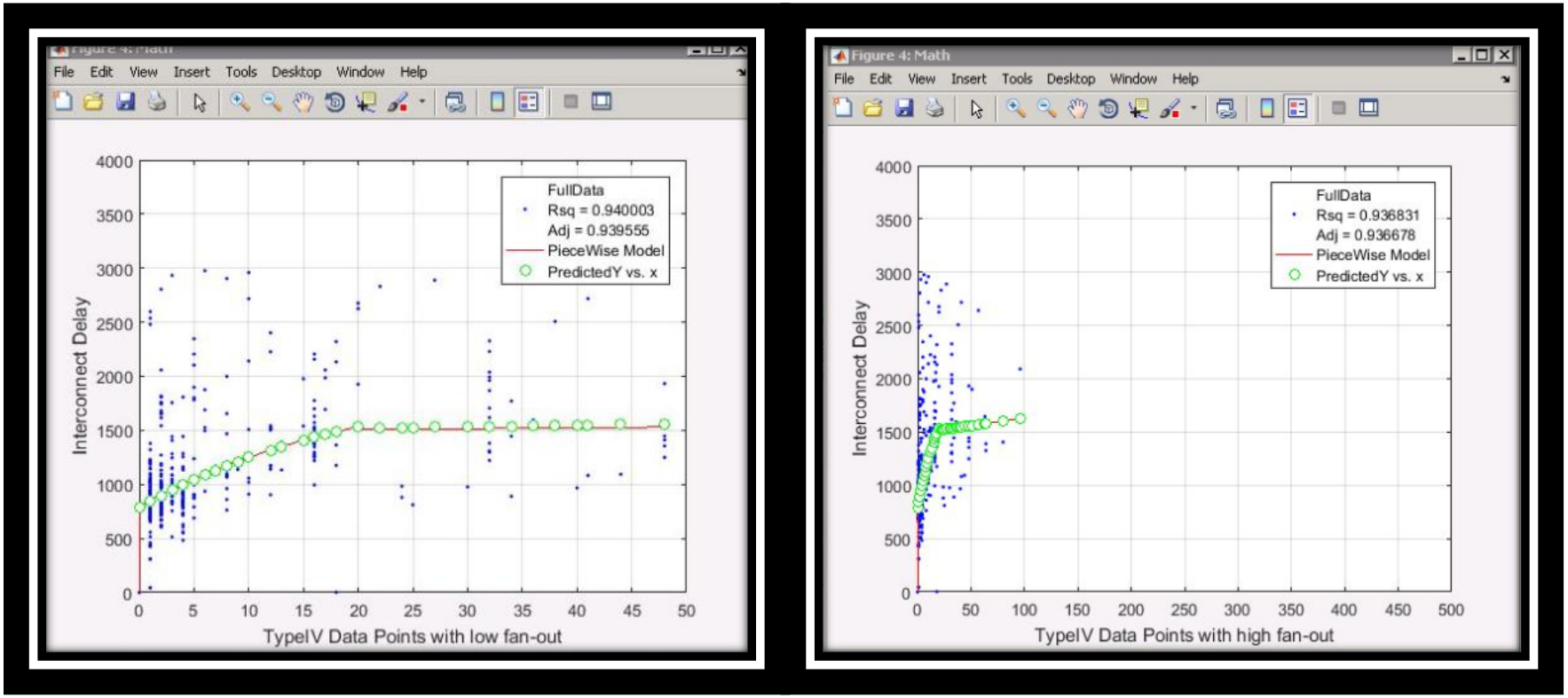
Results (6 of 7)

- Circuit delay prediction model for Type V (URAM IP Block) Data Points:



Results (7 of 7)

- Circuit delay prediction model for Type VI (MATH IP Block) Data Points:



Conclusions

- Using the curve fitting toolbox of MATLAB, we obtain a strong correlation between pre-layout & post-layout timing.

Thank You

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