

MathWorks
**AUTOMOTIVE
CONFERENCE 2023**
Europe

Streamline Automotive SPICE® Compliance Using Model-Based Design

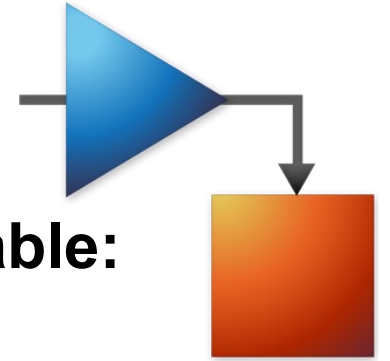
*Mohammad Abu-Alqumsan,
MathWorks*



*Marc Segelken,
MathWorks*



Key Takeaways



Model-Based Design and Model-Based Systems Engineering enable:

- 1. Fast development and realization** of system and software architecture and design
- 2. Early testing** to detect errors in designs and their realization
- 3. Fast and efficient iterations**



Develop **high quality products** following an **efficient Automotive SPICE[®] compliant process**

Automotive SPICE® – Reference Model

Acquisition Process Group (ACQ)

- ACQ.3 Contract Agreement
- ACQ.4 Supplier Monitoring
- ACQ.11 Technical Requirements
- ACQ.12 Legal and Administrative Requirements
- ACQ.13 Project Requirements
- ACQ.14 Request for Proposals
- ACQ.15 Supplier Qualification

Supply Process Group (SPL)

- SPL.1 Supplier Tendering
- SPL.2 Product Release

System Engineering Process Group (SYS)

- SYS.1 Requirements Elicitation
- SYS.2 System Requirements Analysis
- SYS.3 System Architectural Design
- SYS.4 System Integration and Integration Test
- SYS.5 System Qualification Test

Software Engineering Process Group (SWE)

- SWE.1 Software Requirements Analysis
- SWE.2 Software Architectural Design
- SWE.3 Software Detailed Design and Unit Construction
- SWE.4 Software Unit Verification
- SWE.5 Software Integration and Integration Test
- SWE.6 Software Qualification Test

Supporting Process Group (SUP)

- SUP.1 Quality Assurance
- SUP.2 Verification
- SUP.4 Joint Review
- SUP.7 Documentation
- SUP.8 Configuration Management
- SUP.9 Problem Resolution Management
- SUP.10 Change Request Management

Management Process Group (MAN)

- MAN.3 Project Management
- MAN.5 Risk Management
- MAN.6 Measurement

Reuse Process Group (REU)

- REU.2 Reuse Program Management

Process Improvement Process Group (PIM)

- PIM.3 Process Improvement

Primary Life Cycle Processes

Organizational Life Cycle Processes

Supporting Life Cycle Processes

ID:
SYS.5

Name:
System Qualification Test

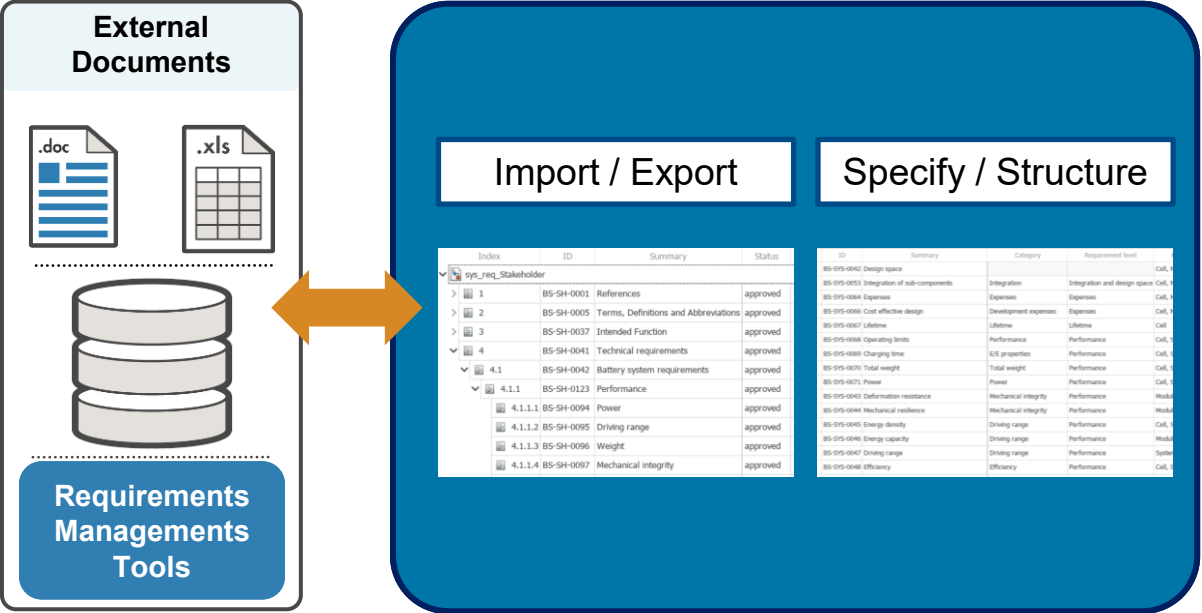
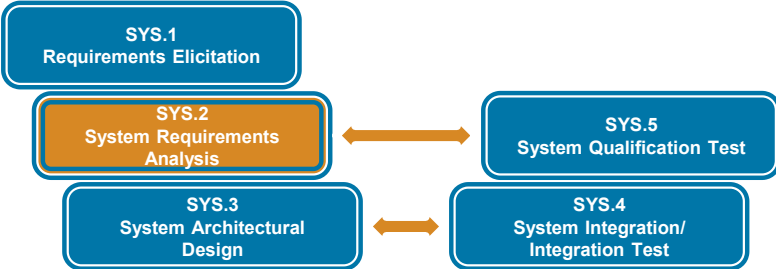
Purpose:

Outcomes:

Base Practices:

Output Work Products:

SYS.2 System Requirements Analysis



Organize, Specify and Customize Requirements with Requirements Toolbox

Organize

	ID	Summary	Category	Requirement level	Keywords
>	sys_req_Stakeholder				
▼	sys_req_BatterySystem				
>	1	BS-SYS-0001	References	Unset	Unset
>	2	BS-SYS-0005	Terms, Difications and Abbreviations	Unset	Unset
>	3	BS-SYS-0037	Intended Function	Unset	Unset
▼	4	BS-SYS-0041	Requirements	Unset	Unset
	4.1	BS-SYS-0042	Design space		Cell, Module, System
	4.1	BS-SYS-0053	Integration of sub-components	Integration	Integration and design space Cell, Module, System
	4.1.1	BS-SYS-0082	Monitoring circuit	Unset	Unset Cell, Module, System
	4.1.1.1	BS-SYS-0119	Voltage measurement rate	E/E properties	Performance Cell, System

Specify

Requirement: BS-SYS-0119

6.19

6.20 ▼ **Properties**

6.21 Type:

6.22 Index: 6.17

6.23 Custom ID:

6.24

6.25 Summary:

4.1.1.1

Description Rationale

Arial 10 **B** *I* U ■ ...

The monitoring circuit shall be able to measure all single-cell voltages at a rate of at least 10 Hz.

Customize

Keywords:

▶ Revision information:

▼ **Custom Attributes**

ASIL:

Category:

Complete:

Correct:

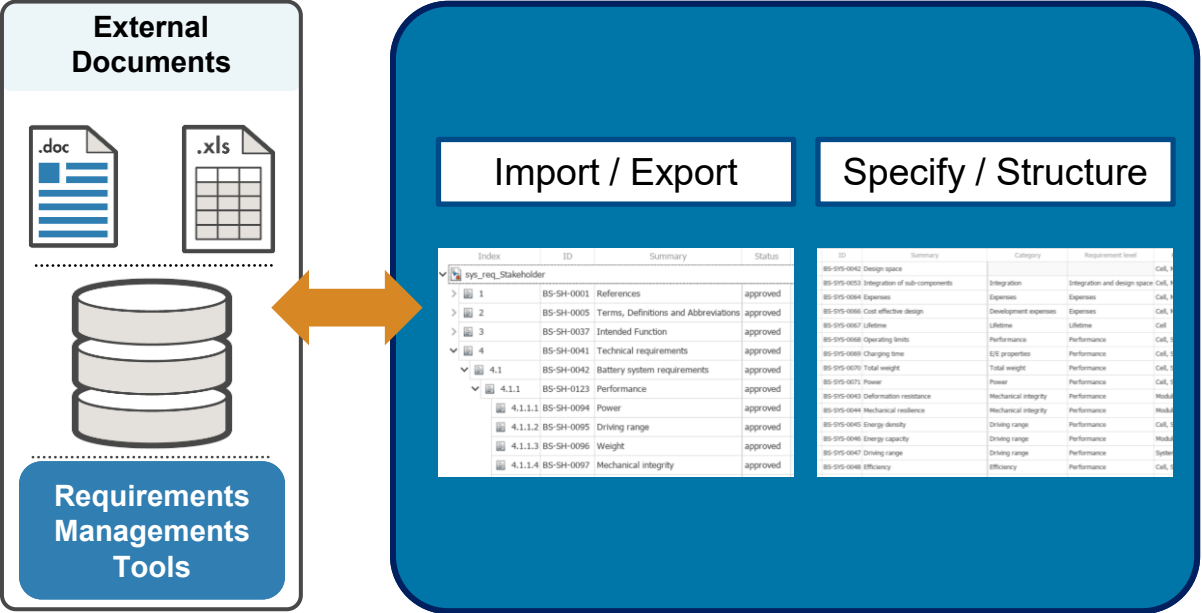
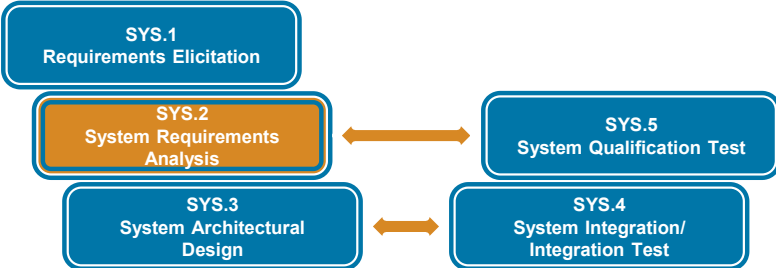
Engineering Domain:

Feasible:

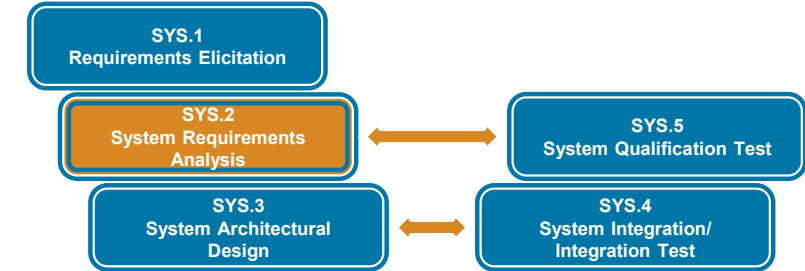
Impact on cost:

Impact on schedule:

SYS.2 System Requirements Analysis



SYS.2 System Requirements Analysis



External Documents

Requirements Management Tools

Import / Export

Specify / Structure

Analyze / Simulate

Index	ID	Summary	Status
sys_req_Stakeholder			
1	BS-SH-0001	References	approved
2	BS-SH-0005	Terms, Definitions and Abbreviations	approved
3	BS-SH-0037	Intended Function	approved
4	BS-SH-0041	Technical requirements	approved
4.1	BS-SH-0042	Battery system requirements	approved
4.1.1	BS-SH-0123	Performance	approved
4.1.1.1	BS-SH-0094	Power	approved
4.1.1.2	BS-SH-0095	Driving range	approved
4.1.1.3	BS-SH-0096	Weight	approved
4.1.1.4	BS-SH-0097	Mechanical integrity	approved

ID	Summary	Category	Requirement level
BS-SH-0042	Design space		Cell, N
BS-SH-0053	Integration of sub-components	Integration	Integration and design space, Cell, N
BS-SH-0044	Expenses	Expenses	Cell, N
BS-SH-0046	Cost effective design	Development expenses	Expenses, Cell, N
BS-SH-0067	Lifetime	Lifetime	Cell
BS-SH-0048	Operating limits	Performance	Performance, Cell, S
BS-SH-0049	Charging time	ES properties	Performance, Cell, S
BS-SH-0070	Total weight	Total weight	Performance, Cell, S
BS-SH-0071	Power	Power	Performance, Cell, S
BS-SH-0043	Deformation resistance	Mechanical integrity	Performance, Modul
BS-SH-0044	Mechanical resilience	Mechanical integrity	Performance, Modul
BS-SH-0045	Energy density	Driving range	Performance, Cell, S
BS-SH-0046	Energy capacity	Driving range	Performance, Modul
BS-SH-0047	Driving range	Driving range	Performance, System
BS-SH-0048	Efficiency	Efficiency	Performance, Cell, S

Coc

Csbu

Tj

Vpp

RPD

$A \Rightarrow B$

CC

Fit

SBU

6

Analyze Logical Requirements with the Requirements Table



Requirements Table: CordLockReqTable_v2/Requirements Table * - Simulink

SIMULATION DEBUG MODELING FORMAT TABLE APPS

Cut Copy Delete Add Requirement Edit Row Append Column Show Columns Delete Column Find Analyze Table Show Report Clear Highlights Stop Time 10.0 Normal Run Stop Fast Restart

Requirements Table

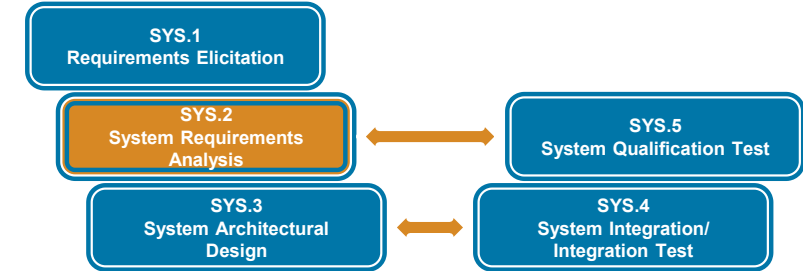
CordLockReqTable_v2 Requirements Table

Requirements Assumptions

Index	Summary	Precondition						Duration	Postcondition LockCommand
		EvseType	ChargeStatus	SessionStopMsg	PilotStatus	ChargePlug	Vinlet		
1	Requirement 1: Lock when evse compatible	Compatible	ChargeStart						Locked
2	Requirement 2: Unlock during normal shutdown		NrmIShutdown	Received			< 60		Unlocked
3	Requirement 3: Unlock during emergency shutdown static pilot		EmrgShutdown		(X == C2) && (X == D2)		< 60		Unlocked
4	Requirement 4: Lock for unsafe voltage					Plugged	>= 60		Locked
5	Requirement 5: Unlock when unplugged					NotPlugged			Unlocked
6	Requirement 6: Unlock during emergency shutdown oscillating pilot		EmrgShutdown		(X == C2) (X == D2)		< 60		Unlocked
7	Requirement 7: Unlock SessionStop not recieved		NrmIShutdown	NotReceived			< 60		Unlocked
8	Requirement 8: Unlock when not charging		NotCharging				< 60		Unlocked
9	Requirement 9: Unlock when compatibility not decided	NotDecided	ChargeStart				< 60		Unlocked
10	Requirement 10: Lock when inlet voltage within range							(-5,250)	Locked

Ready 41% auto(FixedStepDiscrete)

SYS.2 System Requirements Analysis



External Documents

Requirements Management Tools

Import / Export

Specify / Structure

Analyze / Simulate

Index	ID	Summary	Status
sys_req_Stakeholder			
1	BS-SH-0001	References	approved
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3	BS-SH-0037	Intended Function	approved
4	BS-SH-0041	Technical requirements	approved
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4.1.1	BS-SH-0123	Performance	approved
4.1.1.1	BS-SH-0094	Power	approved
4.1.1.2	BS-SH-0095	Driving range	approved
4.1.1.3	BS-SH-0096	Weight	approved
4.1.1.4	BS-SH-0097	Mechanical integrity	approved

ID	Summary	Category	Requirement level
BS-SH-0042	Design space		Cell, N
BS-SH-0053	Integration of sub-components	Integration	Integration and design space, Cell, N
BS-SH-0044	Expenses	Expenses	Cell, N
BS-SH-0046	Cost effective design	Development expenses	Expenses, Cell, N
BS-SH-0067	Lifetime	Lifetime	Cell
BS-SH-0048	Operating limits	Performance	Performance, Cell, S
BS-SH-0049	Charging time	ES properties	Performance, Cell, S
BS-SH-0070	Total weight	Total weight	Performance, Cell, S
BS-SH-0071	Power	Power	Performance, Cell, S
BS-SH-0043	Deformation resistance	Mechanical integrity	Performance, Modul
BS-SH-0044	Mechanical resilience	Mechanical integrity	Performance, Modul
BS-SH-0045	Energy density	Driving range	Performance, Cell, S
BS-SH-0046	Energy capacity	Driving range	Performance, Modul
BS-SH-0047	Driving range	Driving range	Performance, System
BS-SH-0048	Efficiency	Efficiency	Performance, Cell, S

CC

Csbu

Tj

Vpp

RPD

$A \Rightarrow B$

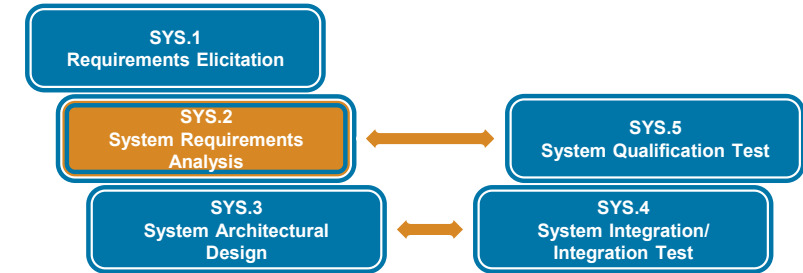
CC

Fit

SBU

8

SYS.2 System Requirements Analysis



External Documents

Requirements Managements Tools

➔

Import / Export

Specify / Structure

Analyze / Simulate

Trace / Check

Index	ID	Summary	Status
>	1	BS-SH-0001 References	approved
>	2	BS-SH-0005 Terms, Definitions and Abbreviations	approved
>	3	BS-SH-0037 Intended Function	approved
>	4	BS-SH-0041 Technical requirements	approved
>	4.1	BS-SH-0042 Battery system requirements	approved
>	4.1.1	BS-SH-0123 Performance	approved
>	4.1.1.1	BS-SH-0094 Power	approved
>	4.1.1.2	BS-SH-0095 Driving range	approved
>	4.1.1.3	BS-SH-0096 Weight	approved
>	4.1.1.4	BS-SH-0097 Mechanical integrity	approved

ID	Summary	Category	Requirement level
BS-SH-0042	Design space	Integration	Integration and design space
BS-SH-0053	Integration of sub-components	Integration	Integration and design space
BS-SH-0064	Expenses	Expenses	Expenses
BS-SH-0066	Cost effective design	Development expenses	Expenses
BS-SH-0067	Lifetime	Lifetime	Life
BS-SH-0068	Operating limits	Performance	Performance
BS-SH-0069	Charging time	ES properties	Performance
BS-SH-0070	Total weight	Total weight	Performance
BS-SH-0071	Power	Power	Performance
BS-SH-0043	Deformation resistance	Mechanical integrity	Performance
BS-SH-0044	Mechanical resilience	Mechanical integrity	Performance
BS-SH-0045	Energy density	Driving range	Performance
BS-SH-0046	Energy capacity	Driving range	Performance
BS-SH-0047	Driving range	Driving range	Performance
BS-SH-0048	Efficiency	Efficiency	Performance

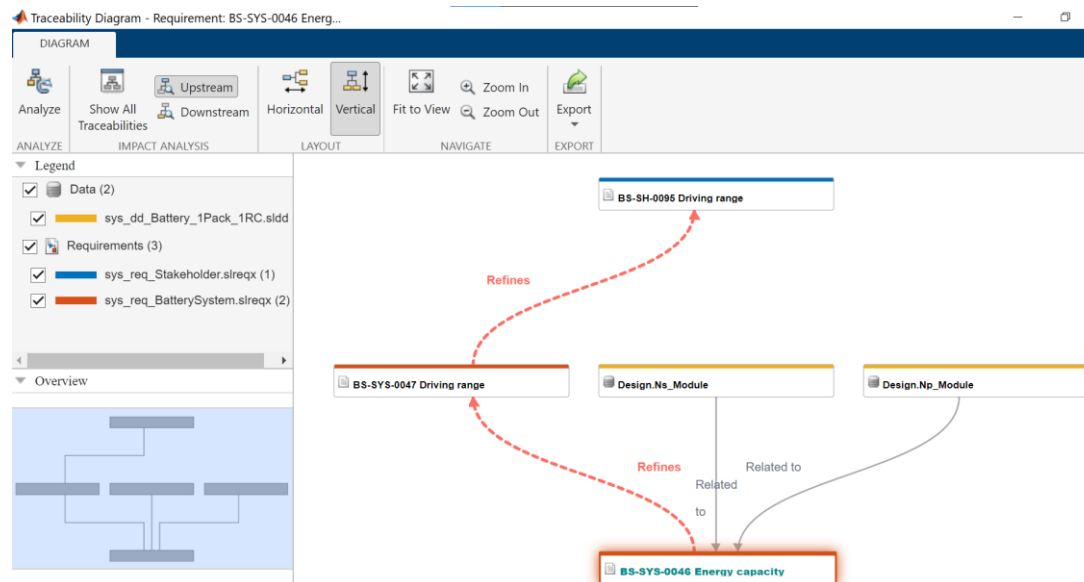
$A \Rightarrow B$

sys_req_Stakeholder	BS-SH-0002 Refer	BS-SH-0003 Reg	BS-SH-0004 Stan	BS-SH-0005 Term	BS-SH-0007 Bank	BS-SH-0018 Bank
sys_req_BatterySystem	BS-SYS-0001 References	BS-SYS-0002 Reference Do	BS-SYS-0003 Regulations	BS-SYS-0004 Standards		

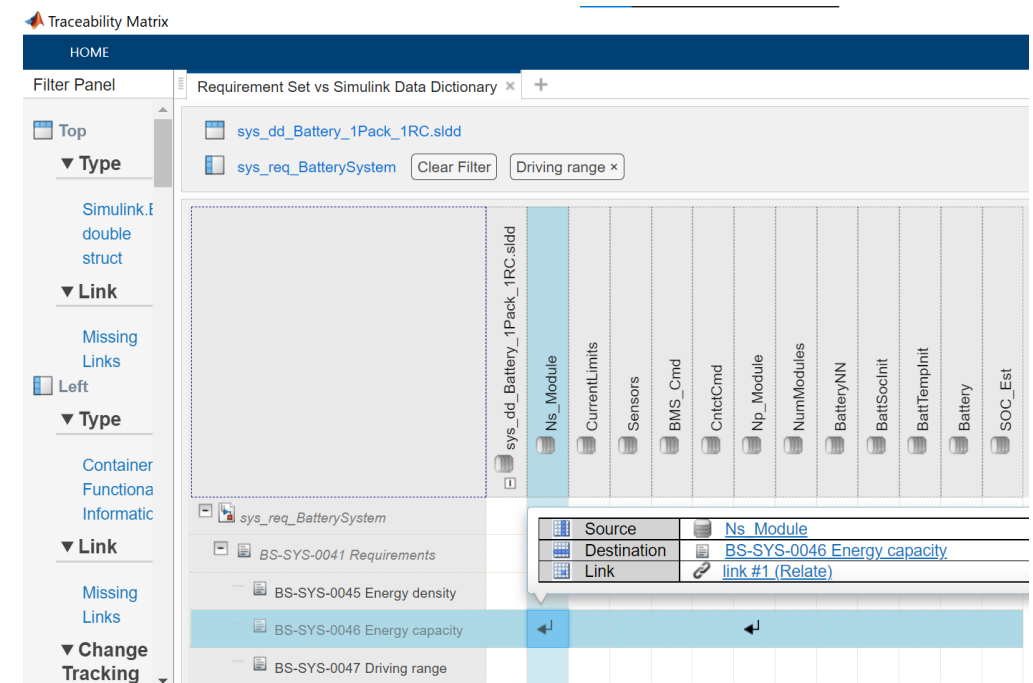
9

Use Traceability Diagrams and Matrixes to Check for Consistency and Completeness

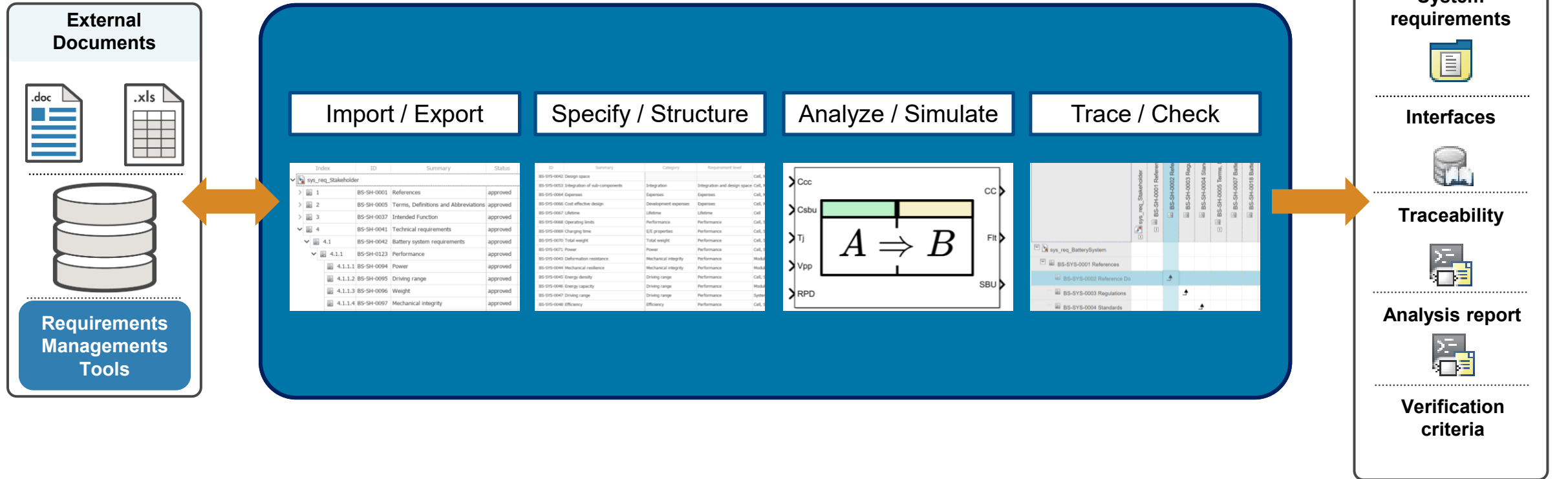
Traceability Diagrams



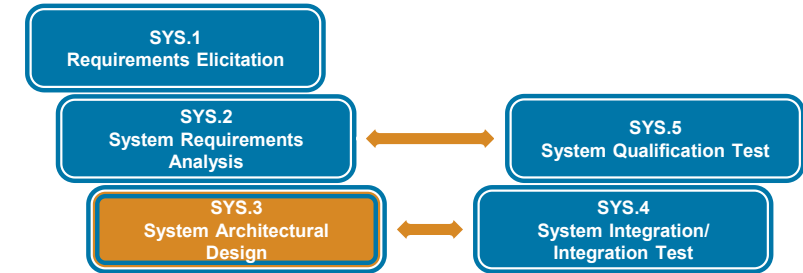
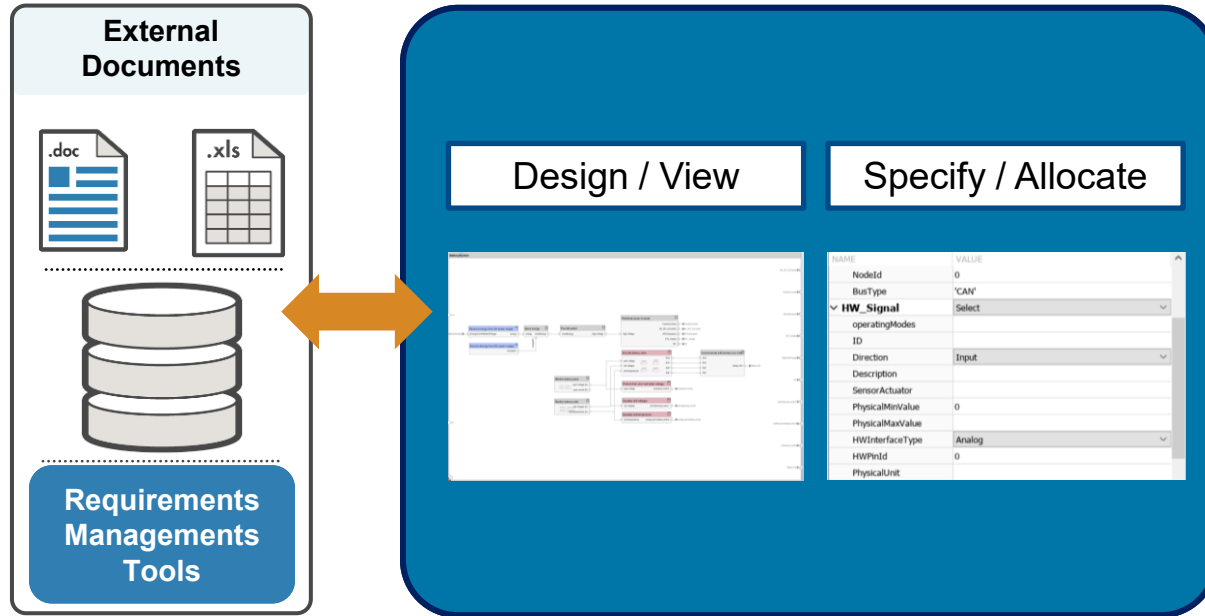
Traceability Matrix



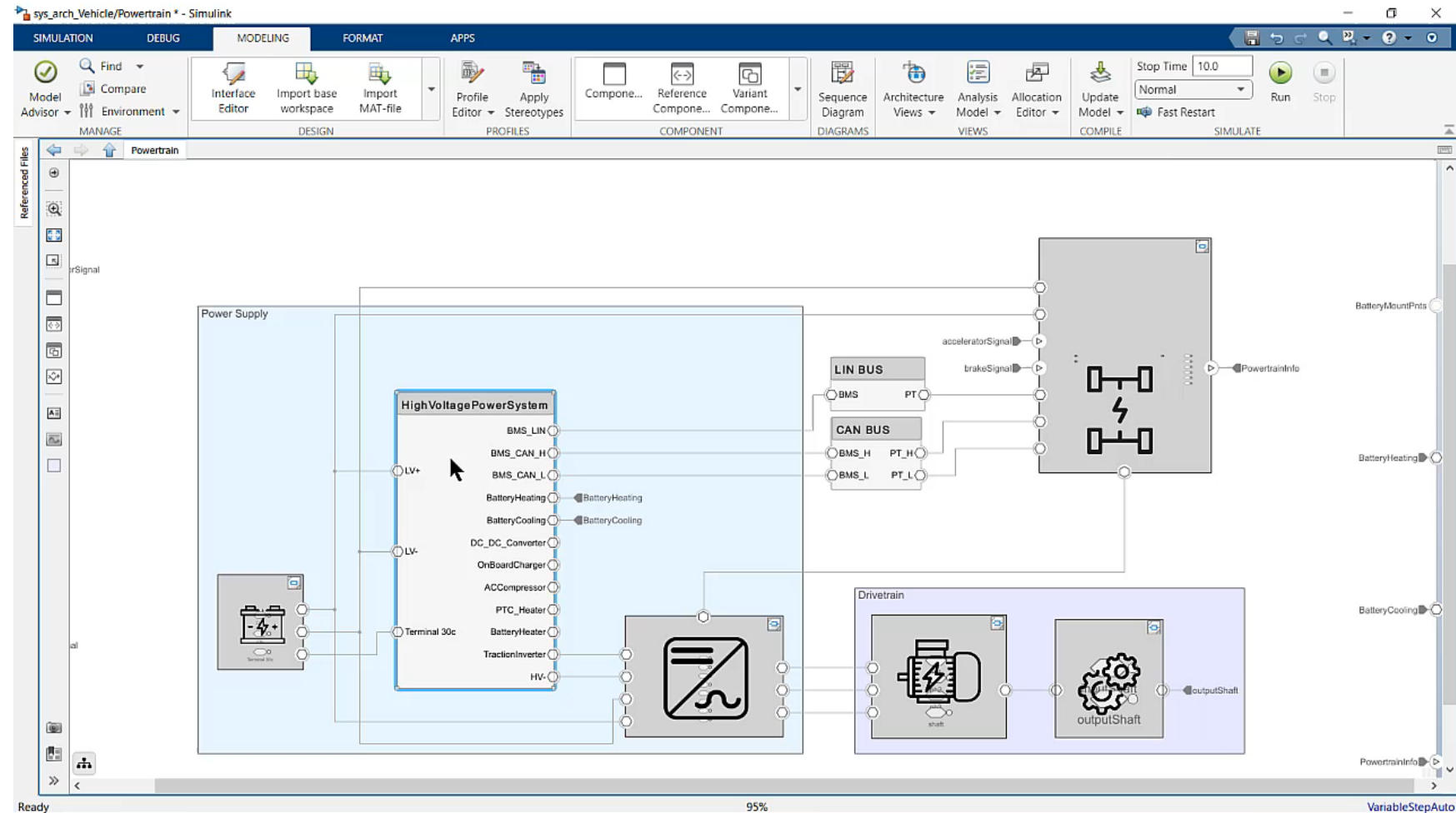
SYS.2 System Requirements Analysis



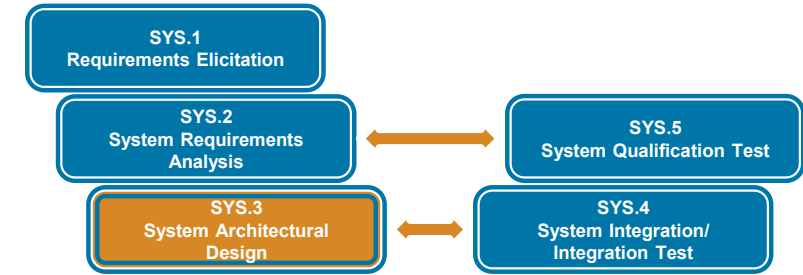
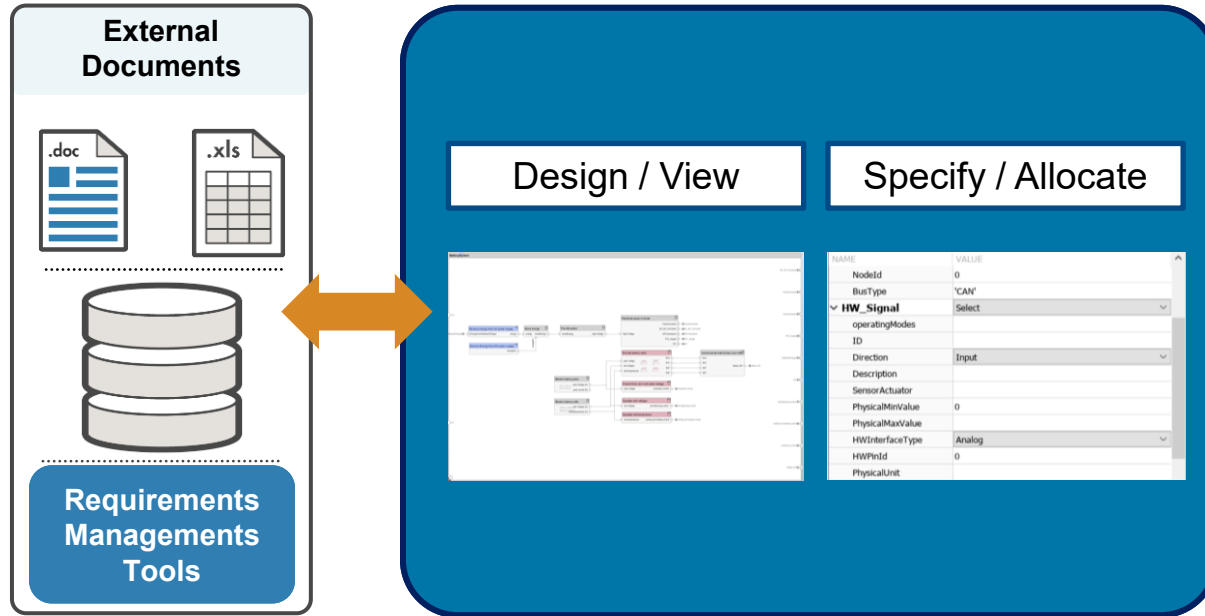
SYS.3 System Architectural Design



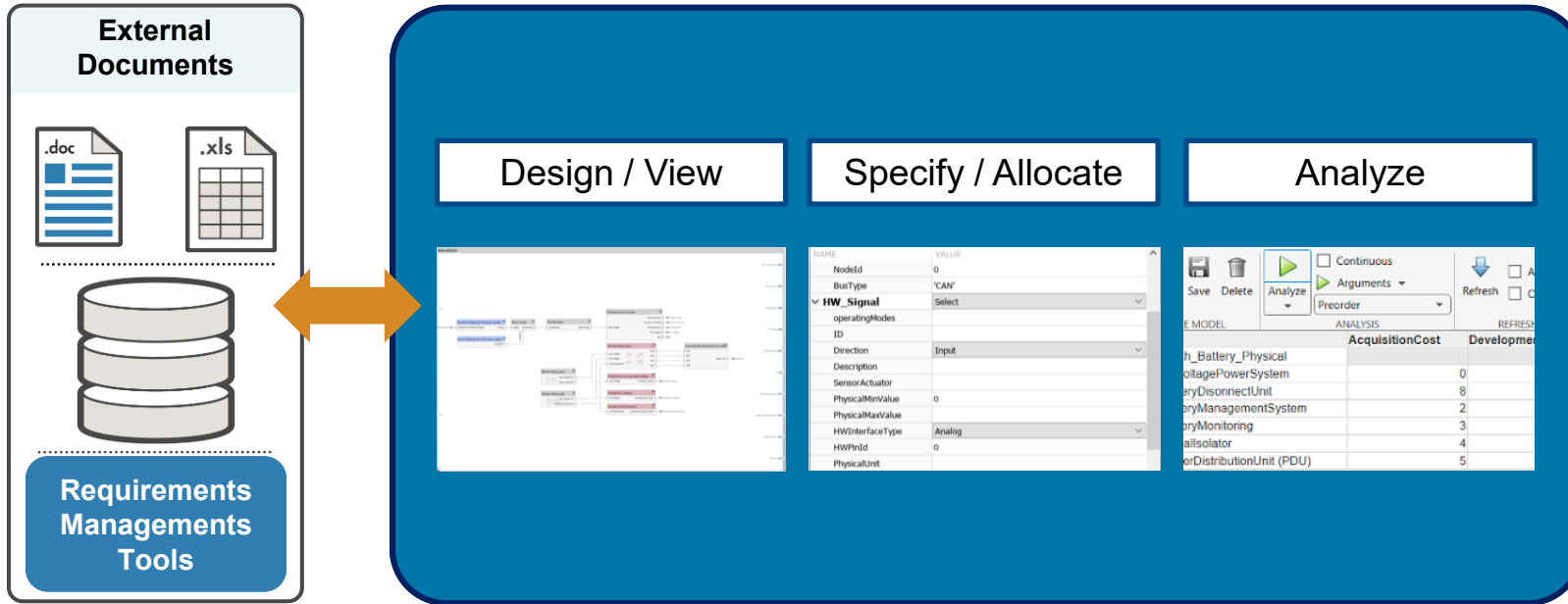
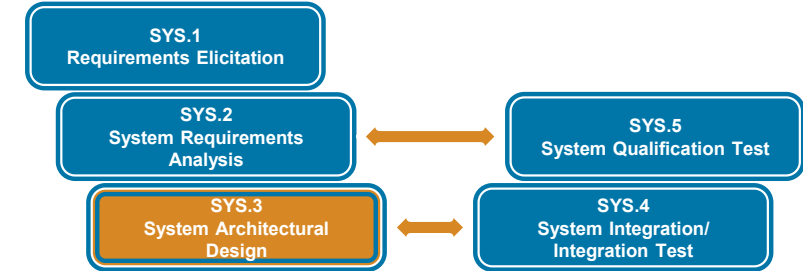
Develop Architectural Design Models with System Composer



SYS.3 System Architectural Design



SYS.3 System Architectural Design



Analyze Architectural Design Models with System Composer

sys_arch_Battery_Physical/HighVoltagePowerSystem - Simulink

SIMULATION DEBUG MODELING FORMAT APPS

Model Advisor Find Compare Interface Editor Import base workspace Import MAT-file Profile Editor Apply Stereotypes Save As Architect... Create Software... Create Simulink... Sequence Diagram Architecture Views Analysis Model Allocation Editor Update Model Fast Restart Run Stop

HighVoltagePowerSystem

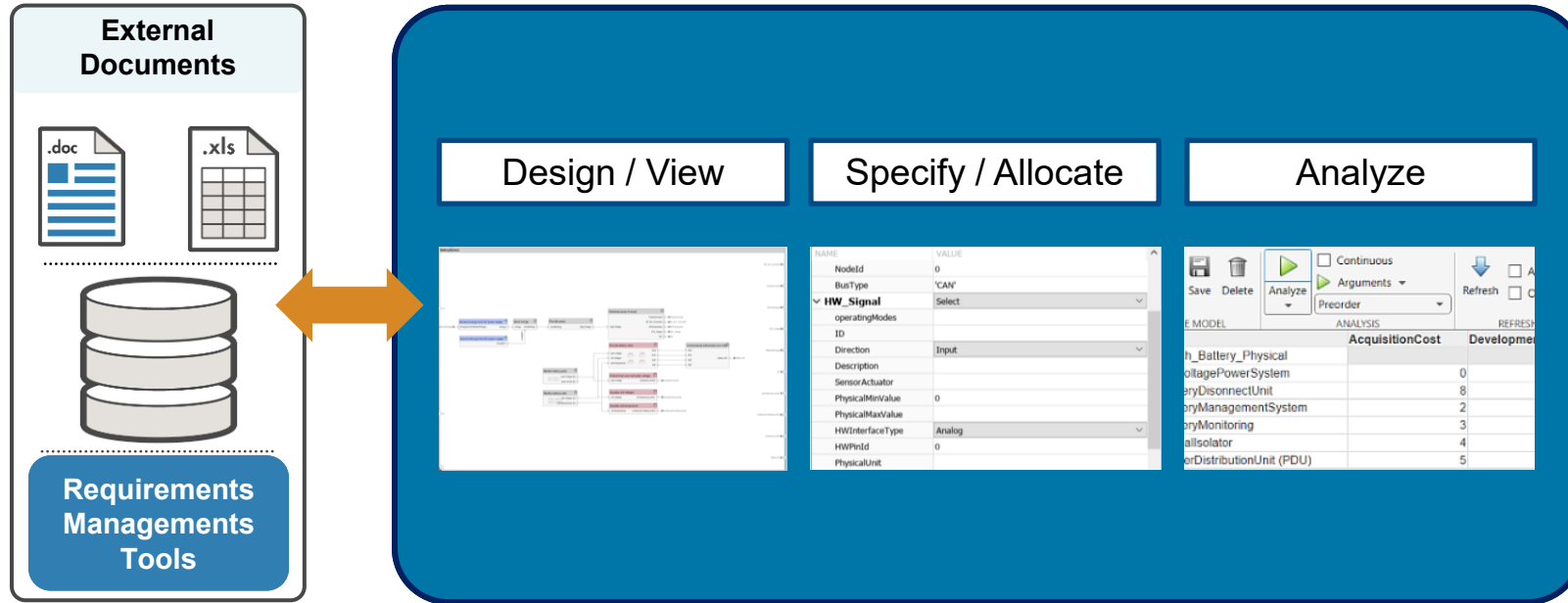
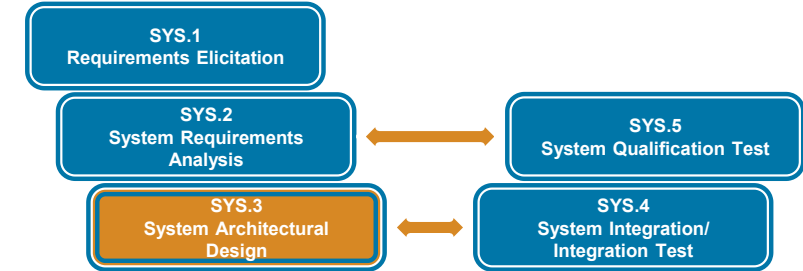
Property Inspector

Component

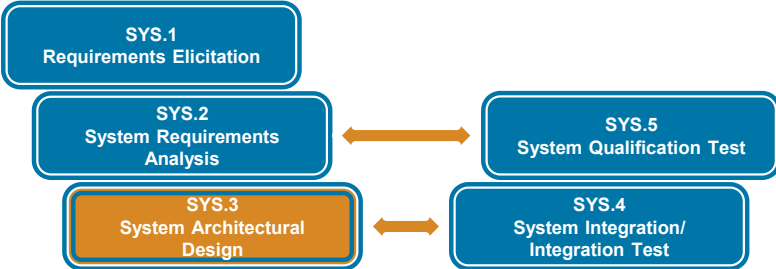
Architecture	Info
NAME	VALUE
▼ Main	
Name	BatteryManagementSystem
Stereotype	Add..
> HW	Select
▼ CapitalCost	
AcquisitionCost	2
IntegrationCost	12
DevelopmentCost	7
TotalCapCost	21
▼ OperationalCost	Select
EnergyCost	17
MaintenanceCost	22
TotalOpCost	39
▼ TotalCost	Select
TotalCost	0
> Parameters	Select

Ready 60% VariableStepAuto

SYS.3 System Architectural Design



SYS.3 System Architectural Design



External Documents

Requirements Managements Tools

➔

Design / View

Specify / Allocate

Analyze

Trace / Check

NAME	VALUE
NodeId	0
BusType	'CAN'
operatingModes	Select
HW_Signal	
ID	
Direction	Input
Description	
Sensor/Actuator	
PhysicalMinValue	0
PhysicalMaxValue	
HWInterfaceType	Analog
HWPinId	0
PhysicalUnit	

	AcquisitionCost	Development
Battery_Physical		
HighVoltagePowerSystem	0	
HighVoltageDisconnectUnit	8	
HighVoltageManagementSystem	2	
HighVoltageMonitoring	3	
HighVoltageIsolator	4	
HighVoltageDistributionUnit (PDU)	5	

- [-] E/E System
 - [-] HV System
 - [-] switch-fuse-box
 - [-] relay / switch box
 - [-] fuse box
 - [-] power cable /busbar

18

Ensure Consistency with Tool Support for Bidirectional Traceability

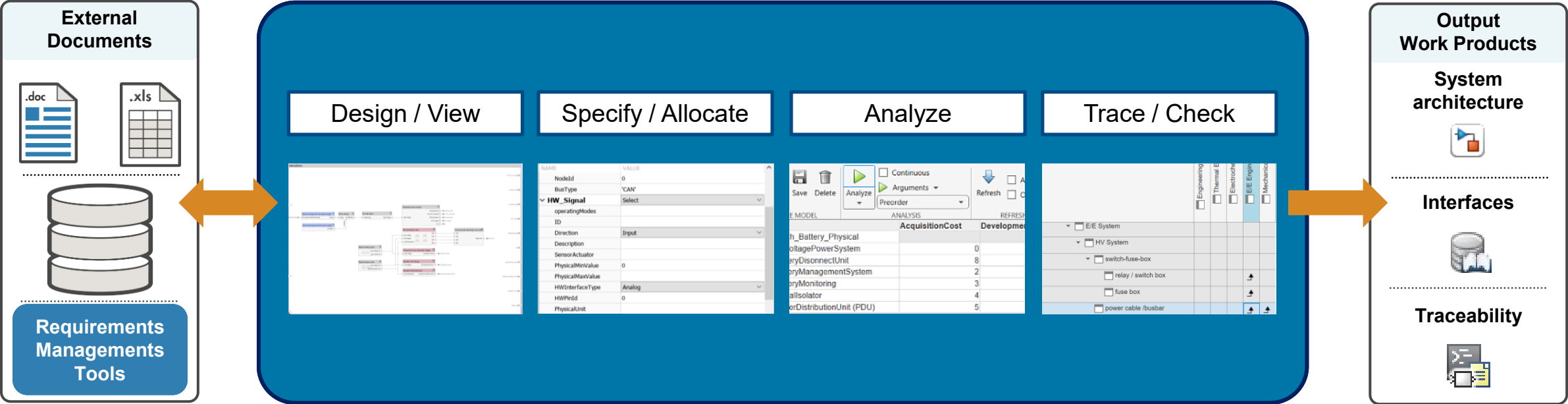
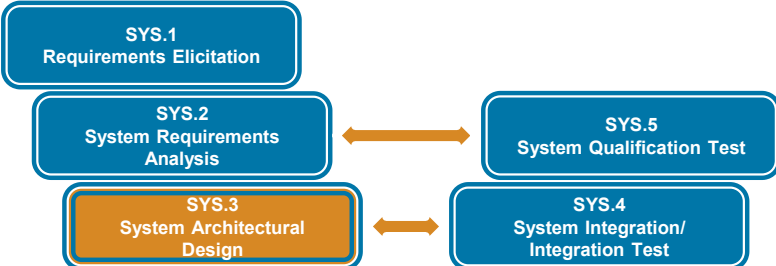
Requirements ↔ Architecture

	sys_arch_Battery_Physical	Battery System	Battery Module	Cell Stack	Battery Cell	electrodes	electrolyte	conductors	separator	Battery Managen	BMS Slave	BMS Master	Tray, Housing (S)	System Cover	Sealing	Pressure Safety ^	Structural Parts	Service-Disconnect	
sys_req_BatterySystem																			
BS-SYS-0001 References																			
BS-SYS-0005 Terms, Difinitions and Abbreviations																			
BS-SYS-0037 Intended Function																			
BS-SYS-0041 Requirements																			
BS-SYS-0043 Design space											↔	↔	↔	↔					↔
BS-SYS-0053 Integration of sub-components											↔	↔	↔				↔		↔
BS-SYS-0064 Expenses					↔	↔	↔	↔			↔	↔	↔	↔	↔	↔	↔	↔	↔
BS-SYS-0066 Cost effective design					↔	↔	↔	↔			↔	↔	↔		↔	↔	↔	↔	↔
BS-SYS-0067 Lifetime											↔	↔	↔	↔	↔	↔	↔	↔	↔
BS-SYS-0068 Operating limits					↔	↔	↔	↔			↔	↔							

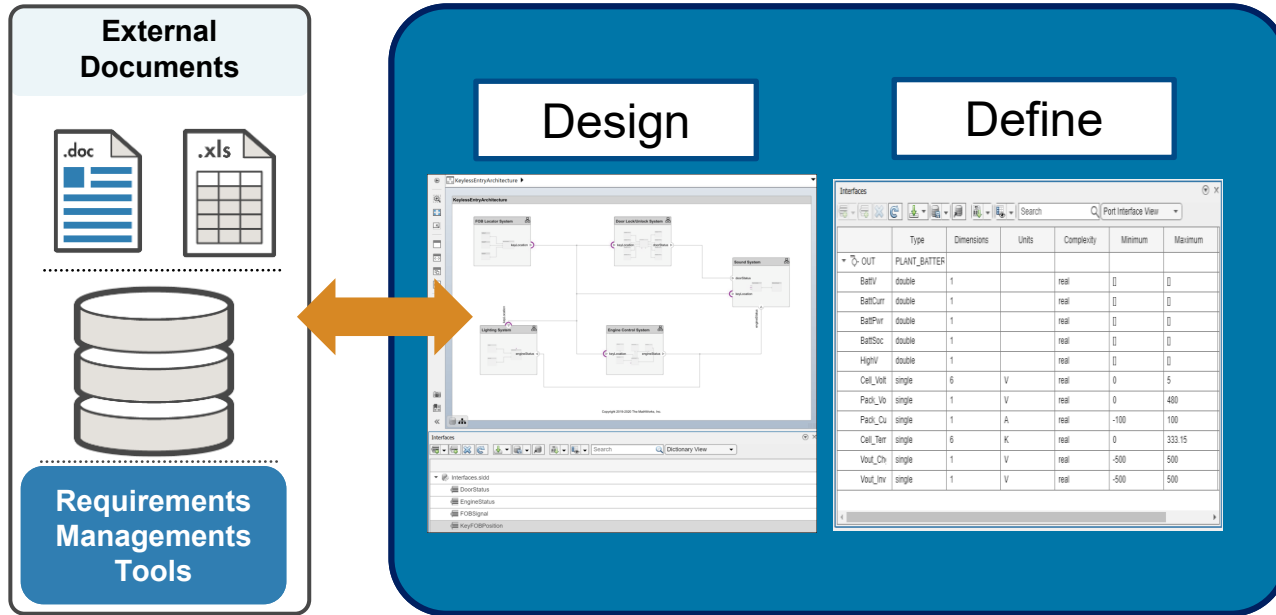
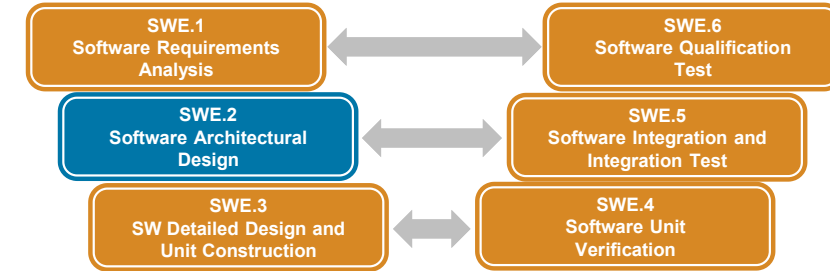
Architecture ↔ Architecture

	sys_arch_Battery_Logical	BatteryPack	BatteryMonitoringUnit	BalancingCircuit	OnBoardCharger	BatteryManagementSystem	CANTransceiver	SafetyContactors	PowerDistributionUnit
sys_arch_Battery_Functional									
BatterySystem									
Communicate Information over CAN							↔		
Monitor battery cells									
Measure cell voltages			↔						
A/D convert cell temperatures			↔						
A/D convert cell voltages			↔						
Measure cell temperatures			↔						
Equalize cell temperature							↔		

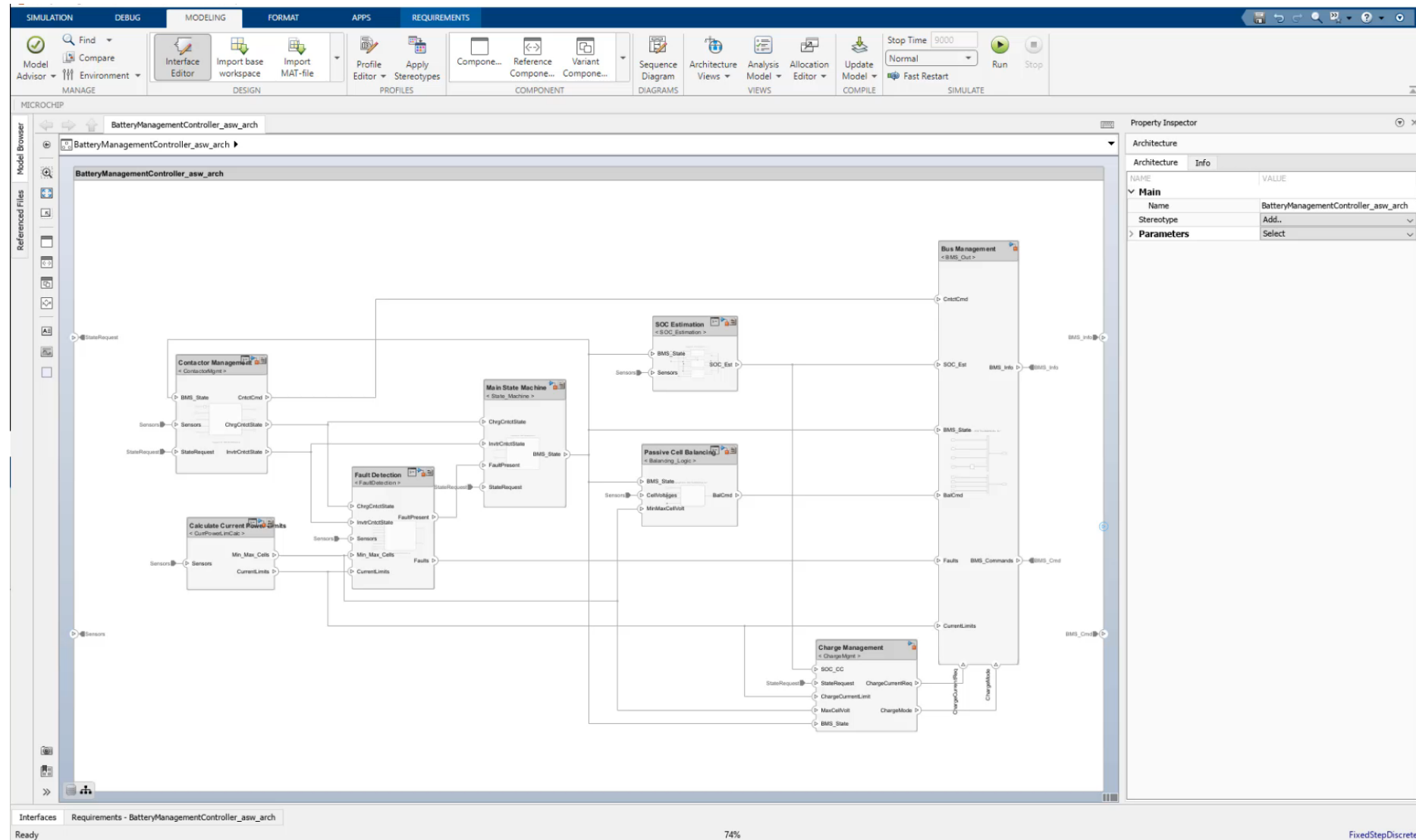
SYS.3 System Architectural Design



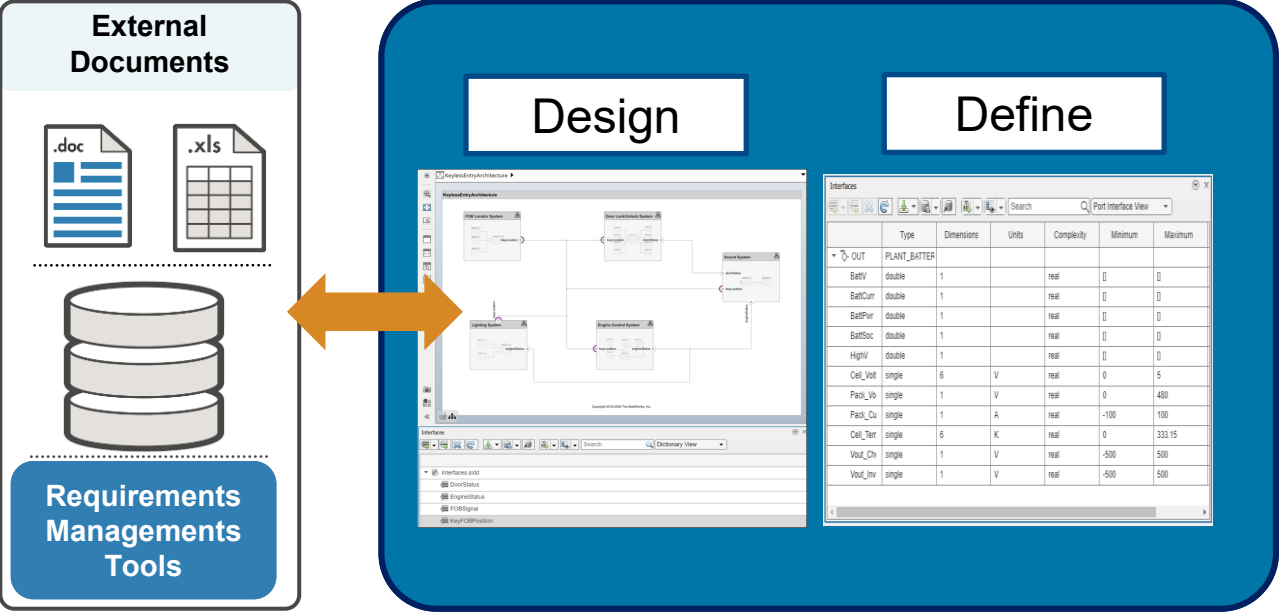
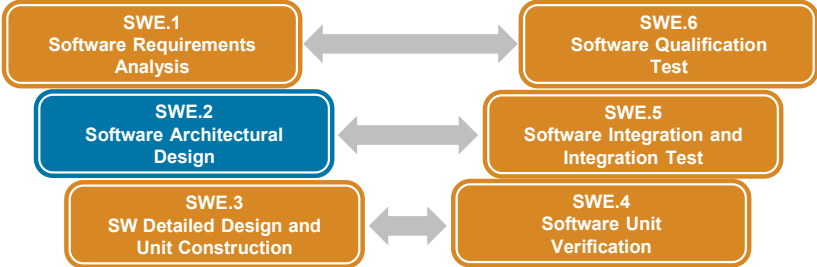
SWE.2 Software Architectural Design



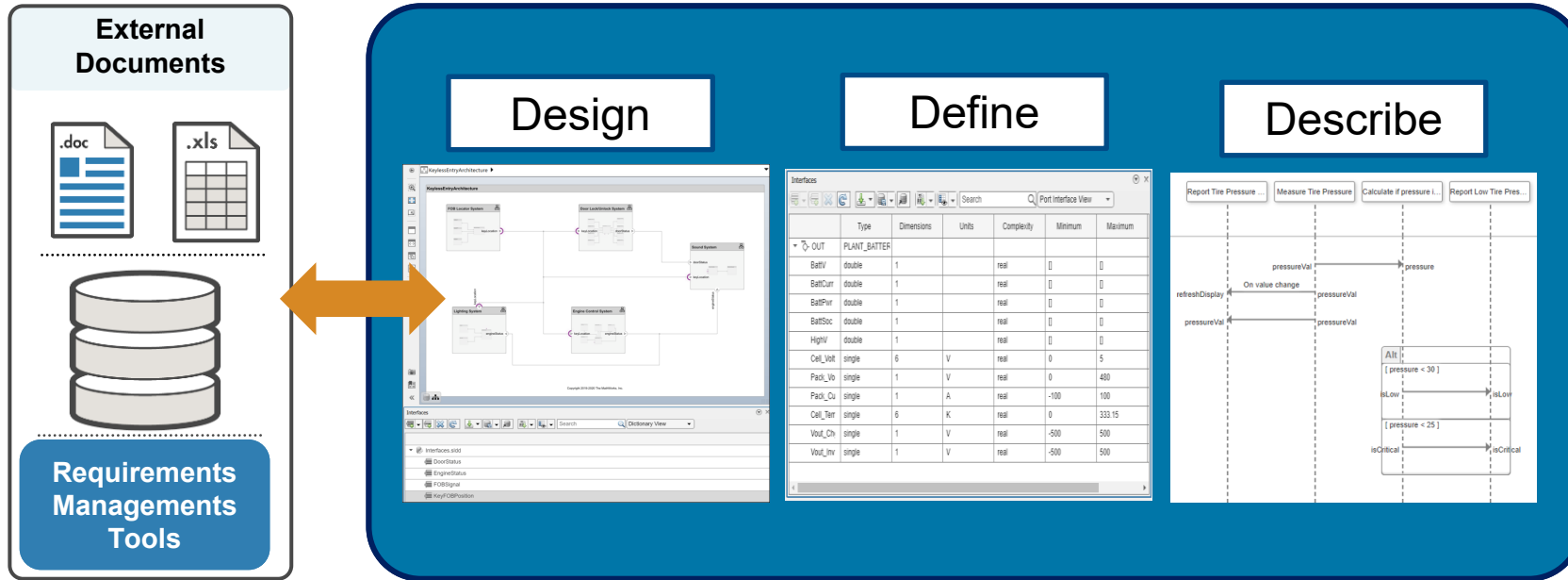
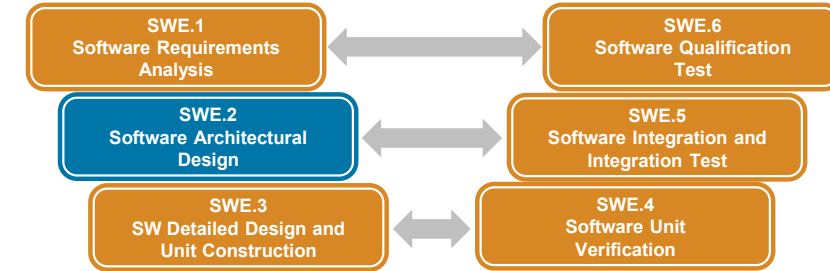
Develop Software Architectural Design



SWE.2 Software Architectural Design



SWE.2 Software Architectural Design



Describe Dynamic Behavior

The screenshot displays the Simulink Model Editor interface for a project named "MICROCHIP". The main workspace shows a state machine diagram for "BatteryManagementController_asw_arch". The diagram includes several components:

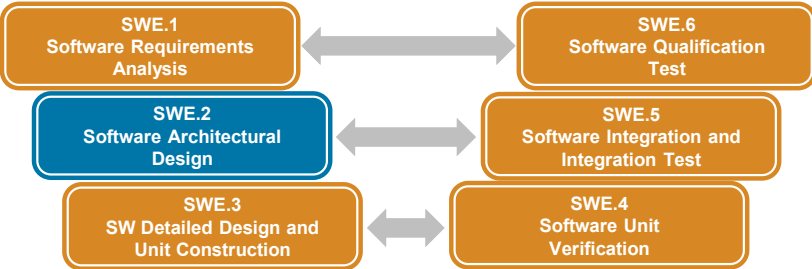
- Main State Machine** (State_Machine): A central state machine component with states like ChrgCntctState, InvtrCntctState, FaultPresent, and StateRequest.
- Fault Detection** (FaultDetection): A component that provides ChrgCntctState, InvtrCntctState, and FaultPresent signals.
- BMS_State** (State_Machine): A component that provides BMS_State and SOC_Est signals.
- Passive Cell Balancing** (Balancing_Logic): A component that provides BMS_State, CellVoltages, and MinMaxCellVolt signals.

The Property Inspector on the right shows the configuration for the selected "Main State Machine" component:

NAME	VALUE
Main	
Name	Main State Machine
Stereotype	Add..
> C_Preliminary_Resourc...	Select
> Parameters	Select

The status bar at the bottom indicates "Ready", "View 1 error", "100%", and "FixedStepDiscrete".

SWE.2 Software Architectural Design



External Documents

Requirements Management Tools

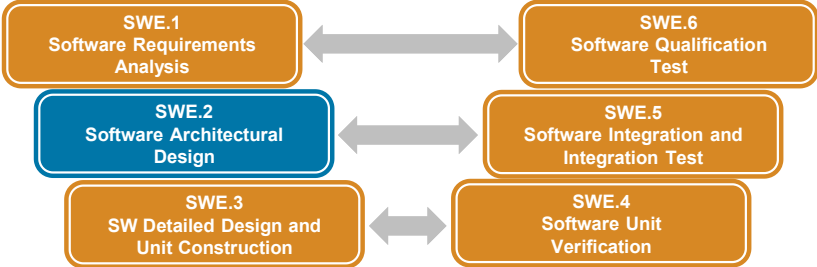
Design

Define

	Type	Dimensions	Units	Complexity	Minimum	Maximum
OUT	PLANT_BATTER					
BattV	double	1		real	0	0
BattCurr	double	1		real	0	0
BattPwr	double	1		real	0	0
BattSoc	double	1		real	0	0
HighV	double	1		real	0	0
Cell_Volt	single	6	V	real	0	5
Pack_Vo	single	1	V	real	0	480
Pack_Cu	single	1	A	real	-100	100
Cell_Tem	single	6	K	real	0	333.15
Vout_Ch	single	1	V	real	-500	500
Vout_Inr	single	1	V	real	-500	500

Describe

SWE.2 Software Architectural Design



External Documents

Requirements Managements Tools

Design

Define

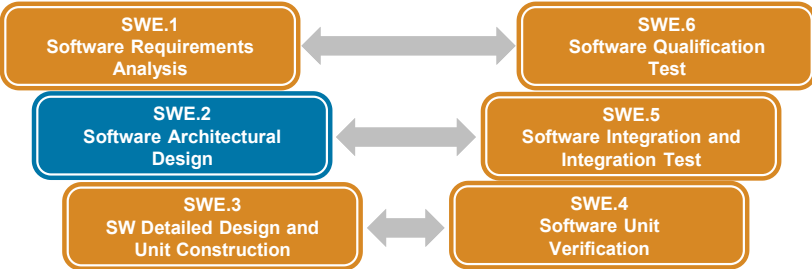
	Type	Dimensions	Units	Complexity	Minimum	Maximum
OUT	PLANT_BATTER					
BattV	double	1		real	0	0
BattCurr	double	1		real	0	0
BattPwr	double	1		real	0	0
BattSoc	double	1		real	0	0
HighV	double	1		real	0	0
Cell_Volt	single	6	V	real	0	5
Pack_Vo	single	1	V	real	0	480
Pack_Cu	single	1	A	real	-100	100
Cell_Ter	single	6	K	real	0	333.15
Vout_Ch	single	1	V	real	-500	500
Vout_Inr	single	1	V	real	-500	500

Describe

Evaluate

ECU	Select
ID	'ED1243'
Part_Number	'C124322'
Supplier	'Supplier_1'
Domain	
Sub_Domain	
Cost	0 Euro
Weight	0 Kg

SWE.2 Software Architectural Design



External Documents

Requirements Managements Tools

Design

Define

Describe

Evaluate

	Type	Dimensions	Units	Complexity	Minimum	Maximum
PLANT_BATTER						
BattV	double	1		real	0	0
BattCurr	double	1		real	0	0
BattPwr	double	1		real	0	0
BattSoc	double	1		real	0	0
HighV	double	1		real	0	0
Cell_Volt	single	6	V	real	0	5
Pack_Vo	single	1	V	real	0	480
Pack_Cu	single	1	A	real	-100	100
Cell_Ter	single	6	K	real	0	333.15
Vout_Ch	single	1	V	real	-500	500
Vout_Inr	single	1	V	real	-500	500

ECU	Select
ID	'ED1243'
Part_Number	'C124322'
Supplier	'Supplier_1'
Domain	
Sub_Domain	
Cost	0 Euro
Weight	0 Kg

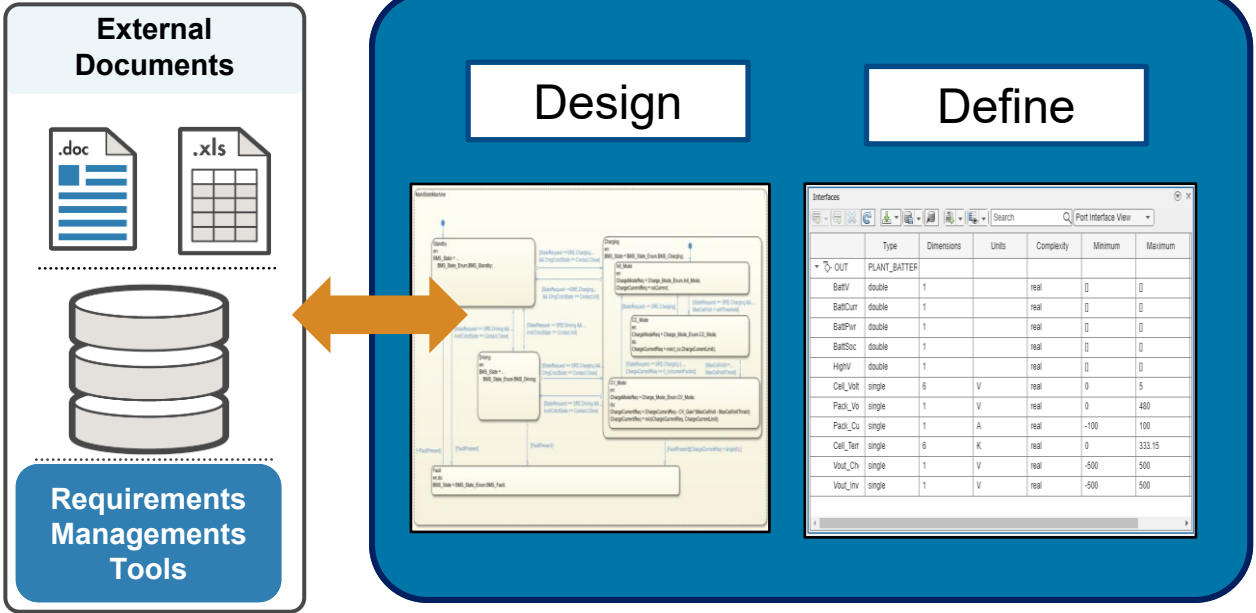
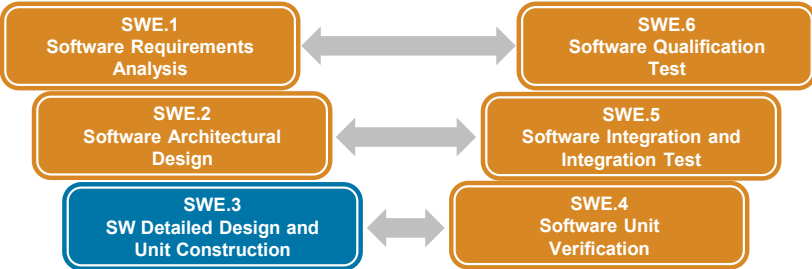
Output Work Products

Software architecture

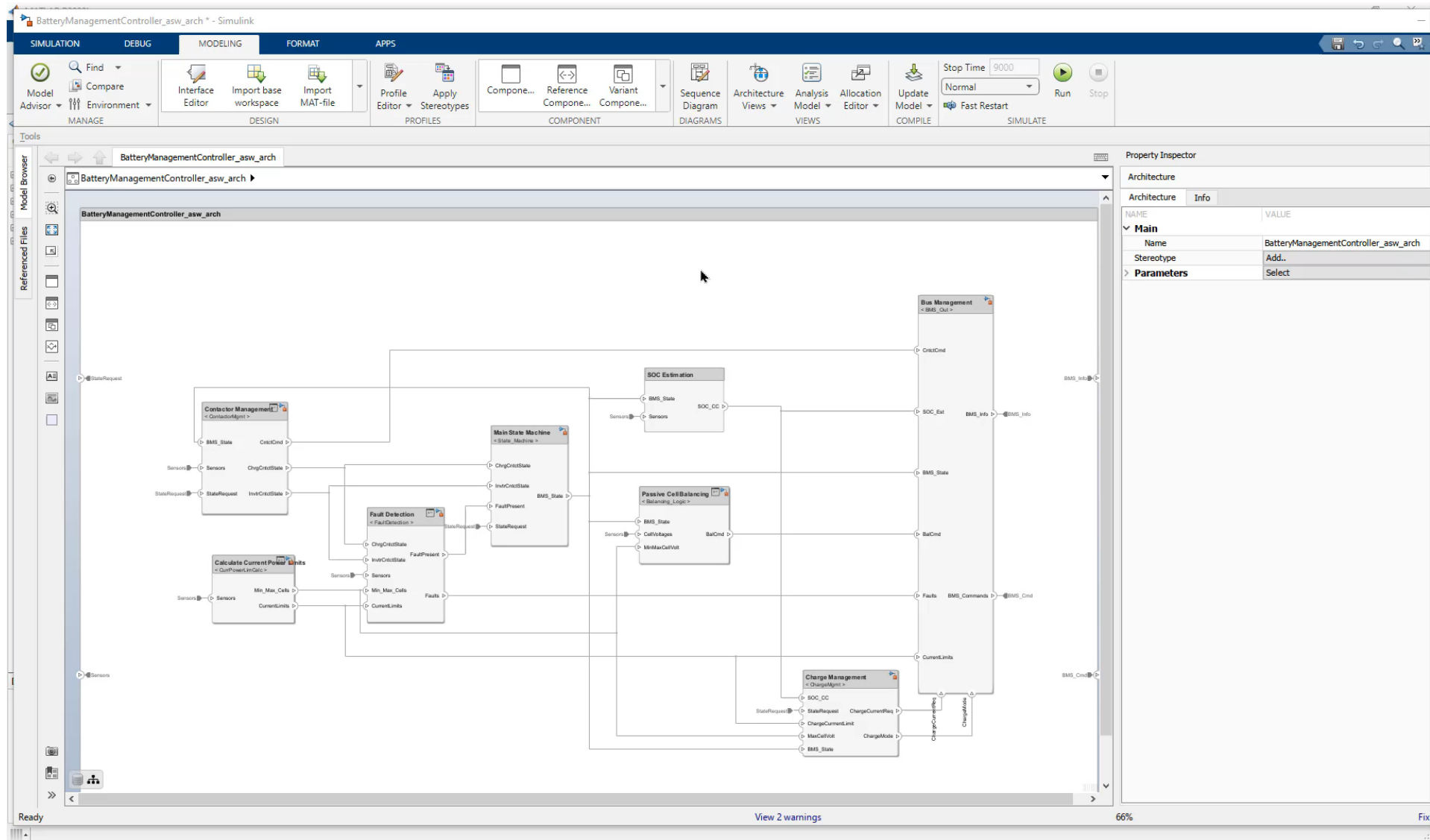
Interfaces

Traceability

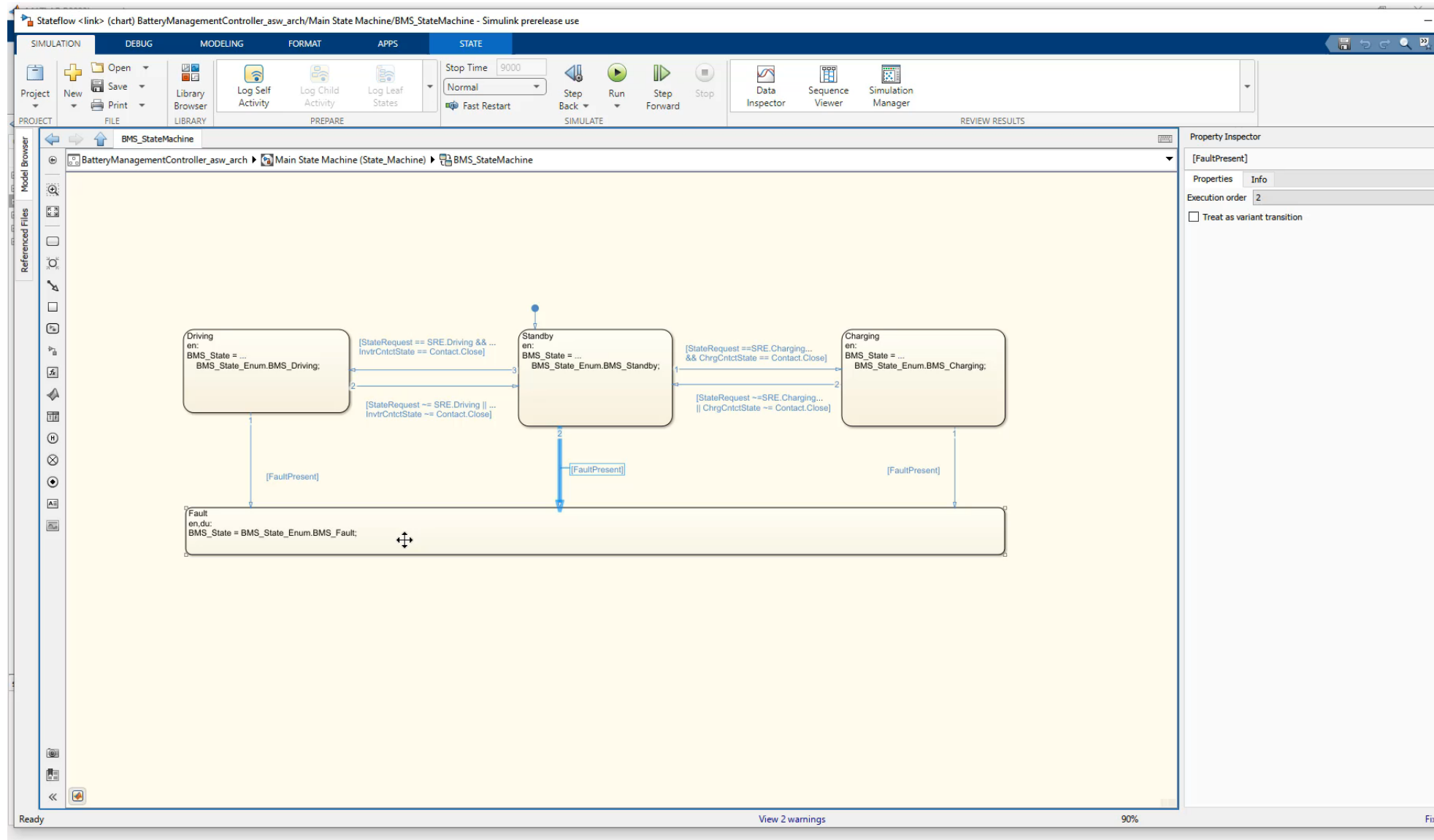
SWE.3 SW Detailed Design and Unit Construction



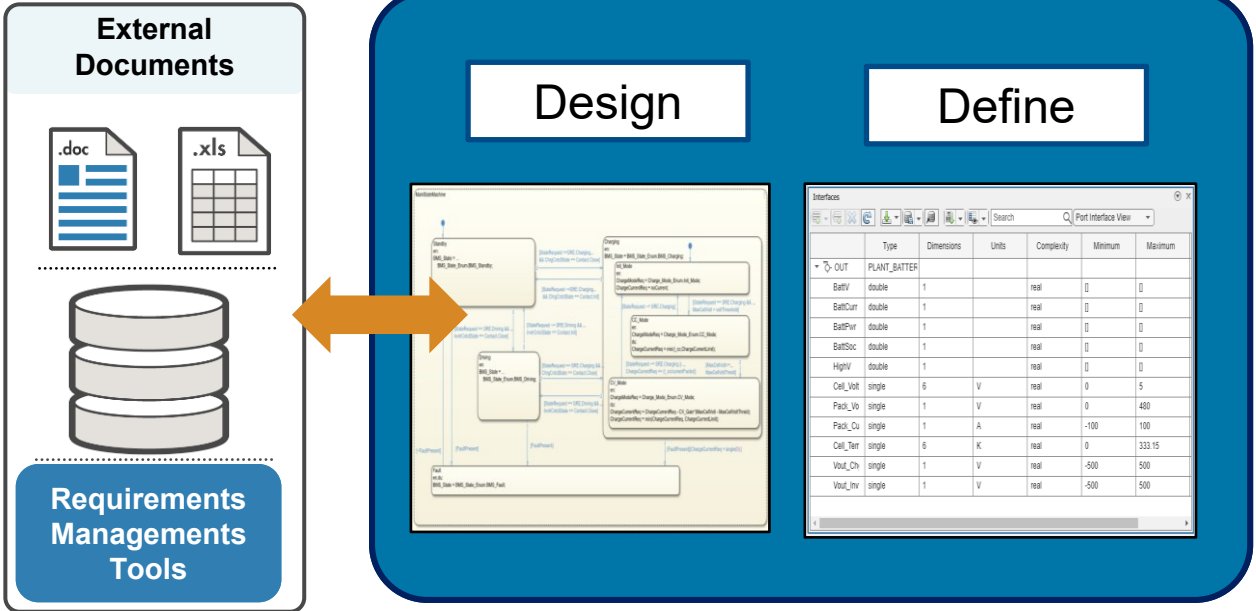
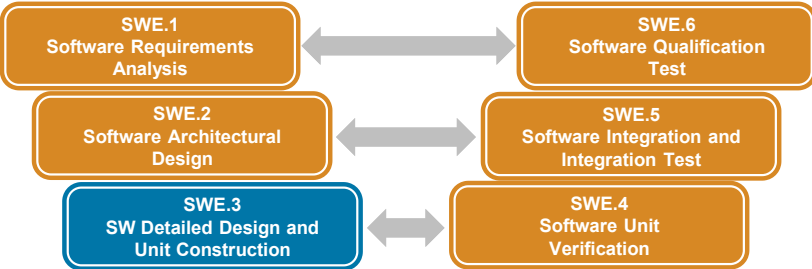
Develop Software Detailed Design



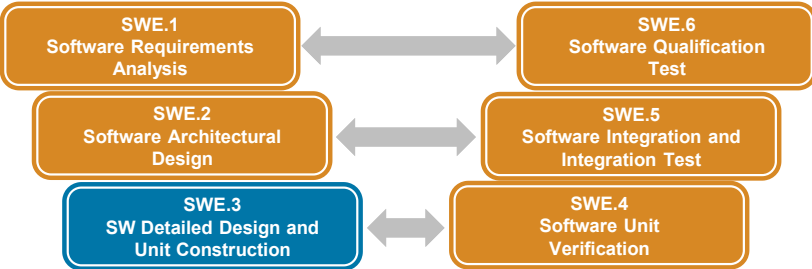
Develop Software Detailed Design



SWE.3 SW Detailed Design and Unit Construction



SWE.3 SW Detailed Design and Unit Construction



External Documents

Requirements Managements Tools

Design

Define

Type	Dimensions	Units	Complexity	Minimum	Maximum
+ OUT PLANT_BATTERY					
BattV	double	1	real	0	0
BattCurr	double	1	real	0	0
BattPwr	double	1	real	0	0
BattSoc	double	1	real	0	0
HighV	double	1	real	0	0
Cell_Volt	single	6	V	real	0 5
Pack_Vo	single	1	V	real	0 480
Pack_Cu	single	1	A	real	-100 100
Cell_Ter	single	6	K	real	0 333.15
Vout_Ch	single	1	V	real	-500 500
Vout_Inv	single	1	V	real	-500 500

Evaluate

Evaluate Software Detailed Design

Dashboard

DASHBOARD

Open Options Legend

MM Model Maintain... MT Model Testing

Collect

Compliant Non-Compliant Warning Uncategorized Report

PROJECT ADD DASHBOARD METRICS OVERLAYS RESULTS

PROJECT - Architecture

MM - State_Machine x MT - State_Machine x

Filter

Name

- CurrPowerLimCalc
- FaultDetection
- SOC_Estimation
- State_Machine
- BMS_SW_Architecture
- sys_arch_Battery_Functional
- sys_arch_Battery_Logical
- sys_arch_Battery_Physical
- sys_arch_Battery_Physical_Hei...
- sys_arch_Battery_VirtualPrototype
- sys_arch_Vehicle
- Battery_Model

ARTIFACTS - Digital Thread

Filter

Name

- State_Machine
 - Functional Requirements
 - Implemented
 - swe_req_BatteryManage...
 - [BS-BMC-SW-2-1-1] I...
 - [BS-BMC-SW-2-1-2] I...
 - [BS-BMC-SW-2-1-3] I...
 - [BS-BMC-SW-2-1-4] I...
 - [BS-BMC-SW-2-2-1] In...
 - [BS-BMC-SW-2-2-2] F...
 - [BS-BMC-SW-2-2-3] F...
 - [BS-BMC-SW-2-2-4] F...

MM Model Maintainability - State_Machine

Updated by: nseghal

Last updated: 9/29/2022, 4:31:01 PM

Component Structure

15

Complexity

4

Depth

6

Breadth

Component Interface

4

Input Ports

1

Output Ports

-

Input Signals

-

Output Signals

Design Cyclomatic Complexity Breakdown

0 200

	Complexity	Distribution
Simulink	1	
Stateflow	15	
MATLAB	0	

Simulink Architecture

0 200

	Count	Distribution
Blocks	1	
Signal Lines	5	
Gotos	0	

Stateflow Architecture

0 200

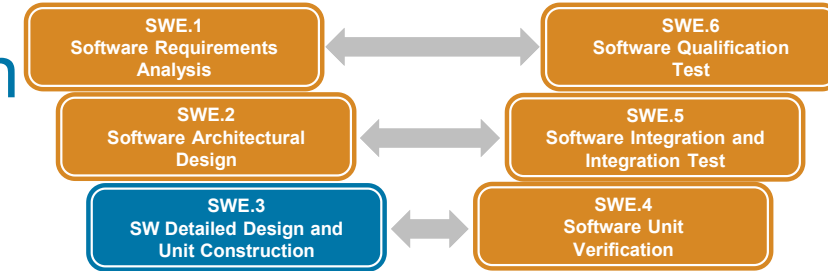
	Count	Distribution
Transitions	8	
States	4	

MATLAB Architecture

0 200

	Count	Distribution
Lines of Code	0	

SWE.3 SW Detailed Design and Unit Construction



External Documents

Requirements Managements Tools

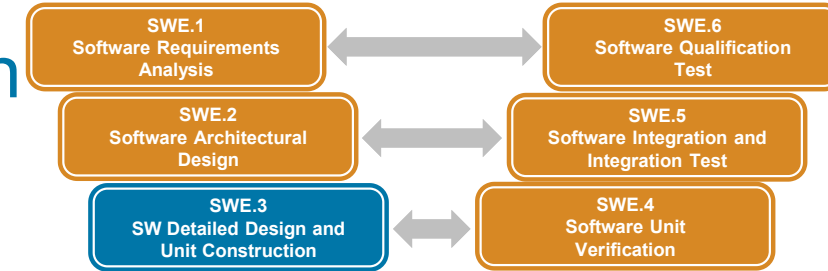
Design

Define

Type	Dimensions	Units	Complexity	Minimum	Maximum
PLANT_BATTERY					
BattV	double	1	real	0	0
BattCurr	double	1	real	0	0
BattPwr	double	1	real	0	0
BattSoc	double	1	real	0	0
HighV	double	1	real	0	0
Cell_Volt	single	6	V	real	0 5
Pack_Vo	single	1	V	real	0 480
Pack_Cu	single	1	A	real	-100 100
Cell_Ter	single	6	K	real	0 333.15
Vout_Ch	single	1	V	real	-500 500
Vout_Inv	single	1	V	real	-500 500

Evaluate

SWE.3 SW Detailed Design and Unit Construction



External Documents

Requirements Managements Tools

Design

Define

Type	Dimensions	Units	Complexity	Minimum	Maximum
PLANT_BATTER			real	0	0
BattV	double	1	real	0	0
BattCurr	double	1	real	0	0
BattPwr	double	1	real	0	0
BattSoc	double	1	real	0	0
HighV	double	1	real	0	0
Cell_Volt	single	6	V	real	0 5
Pack_Vo	single	1	V	real	0 480
Pack_Cu	single	1	A	real	-100 100
Cell_Ter	single	6	K	real	0 333.15
Vout_Ch	single	1	V	real	-500 500
Vout_Inv	single	1	V	real	-500 500

Evaluate

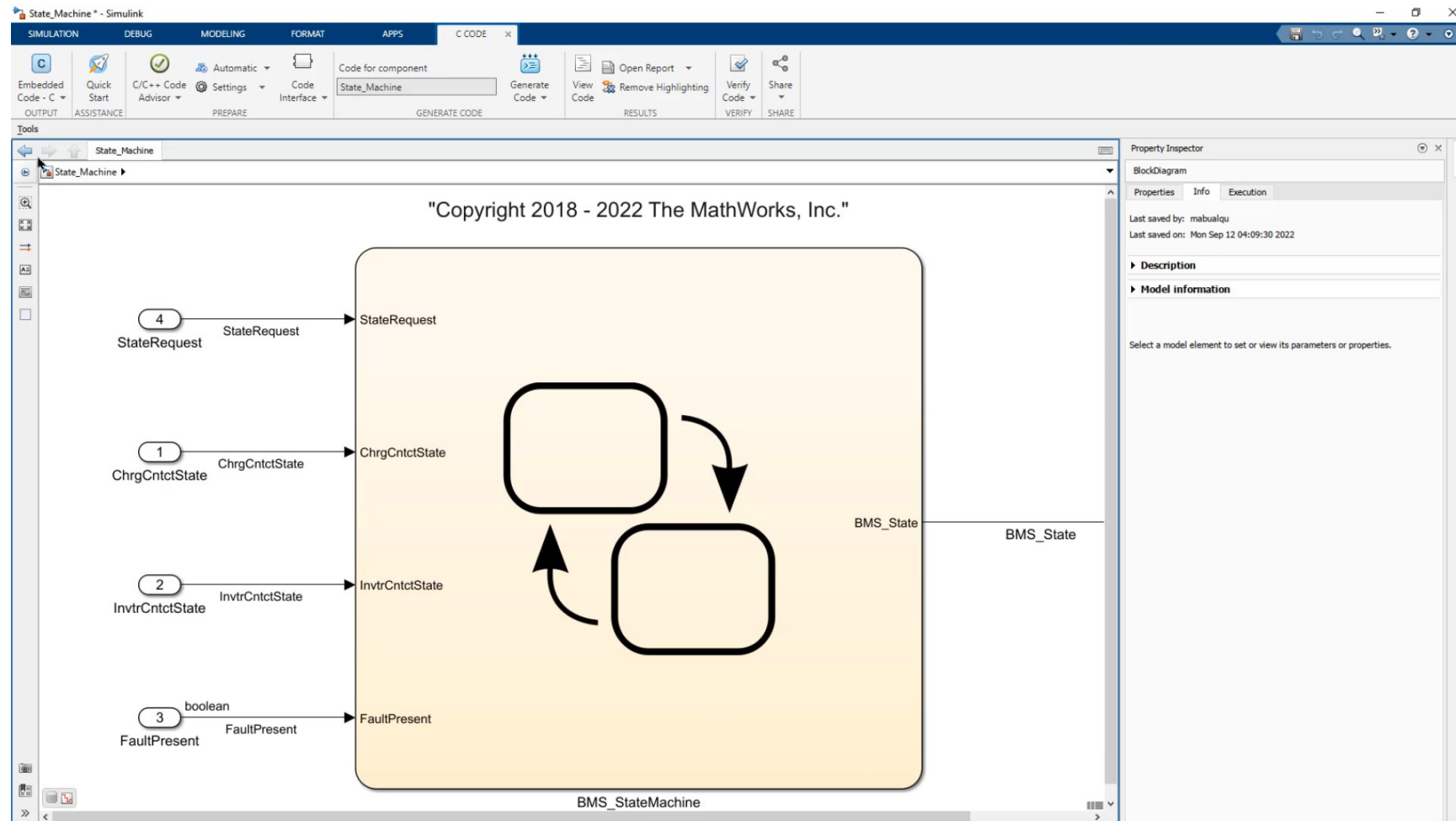
Develop

```

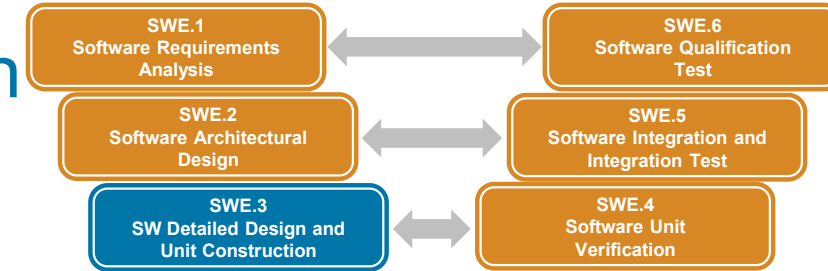
      if ((uint32_T)State_Machine_DW.State_Machine_DW.temporalCount > State_Machine_DW.temporalCountLimit)
      {
        State_Machine_DW.State_Machine_DW.temporalCount = 0;
      }

      if ((uint32_T)State_Machine_DW.State_Machine_DW.is_active_c2 > State_Machine_DW.is_active_c2Limit)
      {
        State_Machine_DW.State_Machine_DW.is_active_c2 = 0;
        *rtu_BMS_State = 0;
        State_Machine_DW.State_Machine_DW.MonitorCurrLi
        State_Machine_DW.State_Machine_DW.MonitorCellVo
        MonitorCellVoltageModeType N
        State_Machine_DW.State_Machine_DW.Delta = (real
        (**rtu_Pack_Voltage) - sum_c
    
```

Develop Software Units



SWE.3 SW Detailed Design and Unit Construction



External Documents

Requirements Managements Tools

Design

Define

OUT	Type	Dimensions	Units	Complexity	Minimum	Maximum
BattV	double	1		real	0	0
BattCurr	double	1		real	0	0
BattPwr	double	1		real	0	0
BattSoc	double	1		real	0	0
HighV	double	1		real	0	0
Cell_Volt	single	6	V	real	0	5
Pack_Vo	single	1	V	real	0	480
Pack_Cu	single	1	A	real	-100	100
Cell_Ter	single	6	K	real	0	333.15
Vout_Ch	single	1	V	real	-500	500
Vout_Inv	single	1	V	real	-500	500

Evaluate

Develop

```

        if ((uint32_T)State_Machine_DW.
            State_Machine_DW.temporalCount
            State_Machine_DW.temporalCou
        )
        if ((uint32_T)State_Machine_DW.
            State_Machine_DW.is_active_c2
            State_Machine_DW.is_MainStateM
            *rty_BMS_State = 0;
            State_Machine_DW.MonitorCurrLi
            State_Machine_DW.MonitorCellVo
            MonitorCellVoltageModeType N
            State_Machine_DW.Delta = (real
            (**rtu Pack Voltage) - sum_c
        
```

Output Work Products

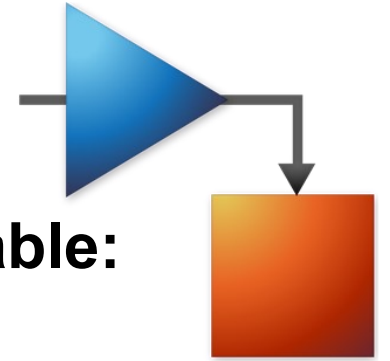
Detailed Design Dynamic Behavior Software Unit

Interfaces

Traceability

Concluding Remarks

Key Takeaways



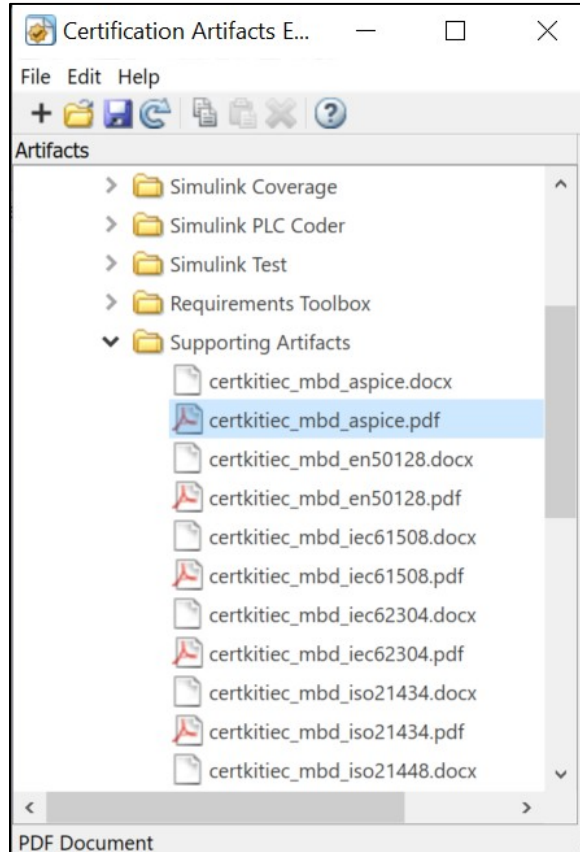
Model-Based Design and Model-Based Systems Engineering enable:

- 1. Fast development and realization** of system and software architecture and design
- 2. Early testing** to detect errors in designs and their realization
- 3. Fast and efficient iterations**



Develop **high quality products** following an **efficient Automotive SPICE[®] compliant process**

IEC Certification Kit – MBD Process for A-SPICE®



IEC Certification Kit Reference Model-Based Design Process for Automotive SPICE®

R2022a

2 System Process Group (SYS)

SYS.1 Requirements Elicitation

Base Practice	Measure	Recommended Tool or Functionality	Work Product [Artifacts]
SYS.1.BP1: Obtain stakeholder requirements and requests	Requirements Toolbox can be used to author and exchange (e.g., through ReqIF) requirements. Requirements can trace back to external documents (e.g., .docx, PDF, or .xlsx).	Requirements Toolbox System Composer	Customer requirements [Requirements files, generated reports from requirements and models]

3 Software Engineering Process Group (SWE)

SWE.1 Software Requirements Analysis

Base Practice	Measure	Recommended Tool or Functionality	Work Product [Artifacts]
SWE.1.BP1: Specify software requirements	The Requirements Toolbox can be used to author and exchange (e.g., through ReqIF) software requirements. You can also link textual system requirements to system requirements. Additionally, software requirements can trace back to external documents (e.g., DOC, PDF, Excel). System Composer can be used to define semi-formal notations (e.g., sequence diagrams and state charts) to capture software requirements.	Requirements Toolbox System Composer	System requirements specification Interface requirements specification [Requirements files, generated reports from requirements and models]
SWE.1.BP2: Structure software	Requirements Toolbox can be used to group and categorize software requirements to create a hierarchy.	Requirements Toolbox	Analysis Report [Requirements files, generated reports from requirements and models]

January 7, 2022

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